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FH3D04

SOFTWARE DEFINED QUAD 3D HALL SENSOR

DATASHEET

DATE	21.11.2023
EDITION	1
REVISION	1.00

CHANGELOG

Date / Edition / Revision	Changes
21.11.2023, Edition 1, Revision 1.00	Initial version

0 Content

1
FH3D04 Overview

1.1
General Description

The FH3D04 is a quad 3D Hall sensor based on Fraunhofer HallinOne® technology. This versatile magnetic field sensor uses pure Hall effect principle without magnetizable materials.
FH3D04 offers high dynamic magnetic range and accurate 3D magnetic field measurement at four positions arranged in a square with a pitch of 1.5 mm in a planar IC in a 2.5x2.5x0.6mm WLCSP package with 0.5mm solder ball pitch.
It can be used as a position sensor for linear (axial/orthogonal and axial/parallel) or angular (on-axis and off-axis) movement of permanent magnets, as a current sensor or as a magnetic field probe. Even 3D and up to 6D position measurement for joystick or gimbal applications are possible.
By use of several integrated 3D Hall sensors measurements stray field robust applications can be implemented.

Sensor placement:	Four 3D Hall sensors (also called pixel cells) arranged in a square with a pitch of 1.5 mm. Temperature sensor for system-level drift tracking.
Measurements:	Magnetic field value (X-, Y- or Z-direction) of the activated sensor or temperature signal. Measurement range full scale from ~10 mT up to ~1.5 T. Measurement rate up to 80 kHz at 10 Bit or 1.8 kHz at 16 Bit resolution.
Software defined sensor:	Each sensor element can be independently configured concerning measurement range and rate. The measurement flow (active sensor elements and measurement order) is software defined, too. An OTP contains electrical trim values,
Integrated excitation coil:	Enables magnetic calibration without need for magnetic setup and magnetic self-test during operation.
Communication interface:	The ASSP offers a register based four wire SPI interface with the pins MISO, MOSI, SCK, CS_N and an optional READY signal. The maximum interface clock frequency is 16 MHz. Daisy Chain available on request.
Digital state machine:	The digital state machine consists of • an automatic decimation of the sigma-delta based ADC values • shadow registers as memory for the output values for continuous operation • control for automatic spinning current measurement and offset centring

- sequencer for measuring several sensors without reconfiguration
- diagnostic flags

During normal operation minimum the following functionality has to be implemented for example in an external microcontroller:

- initialization of the ASIC
- sequential control of the measurements (measure x, y, z and temperature) or just readout of sequencer result values
- signal processing
    - sensitivity compensation over temperature
    - offset compensation over temperature

1.2
Block Diagram

The chip consists of four 3D Hall sensors, an excitation coil and its high voltage current source, the analogue signal computation channel with programmable gain amplifier plus offset centering, ΣΔ-Modulator and a decimation register. The state machine controls the sequencer, decimation, offset centering and the 4-phase measurement cycle. The system clock has to be fed in by a dedicated CLK pad.

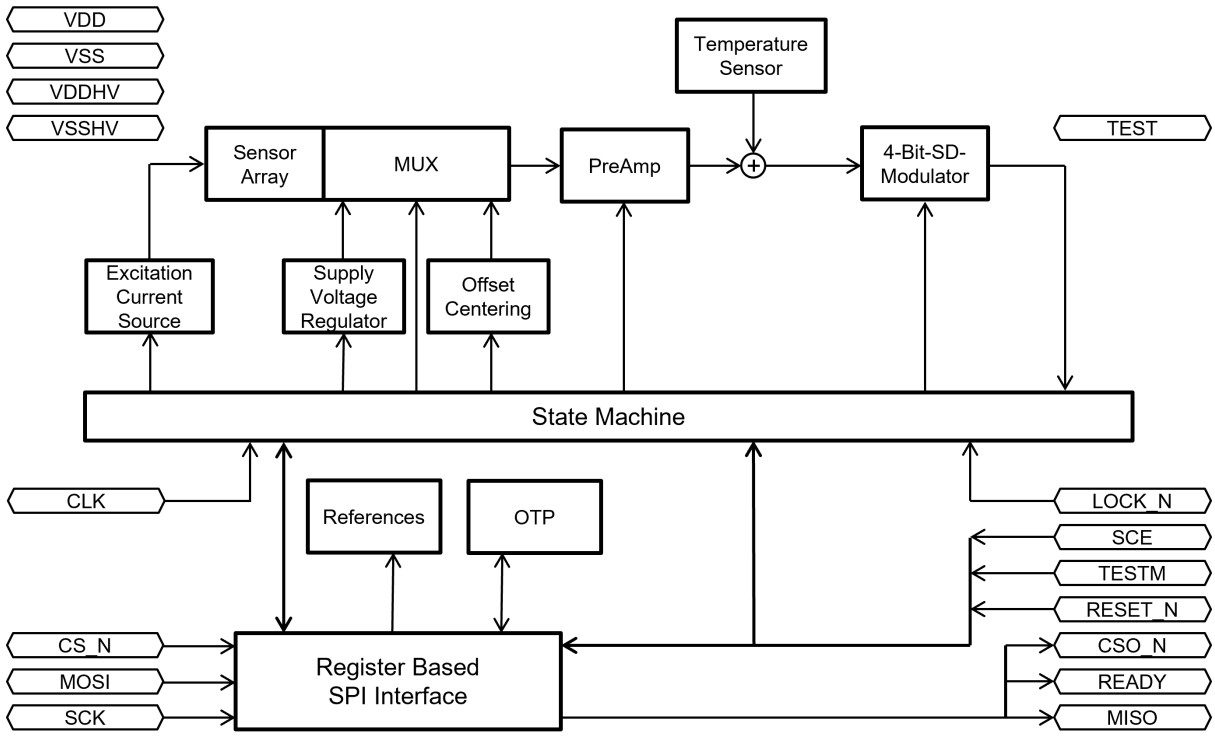

Figure 1: Block diagram

1.3
Customer Support

For questions and troubleshooting please contact the customer support:

Email: contact@lze-innovation.de

2
Characteristics

2.1
Operating Conditions

Table 1: Operating conditions

Parameter	Min.	Typ.	Max.	Unit
Ambient temperature	-40	25	125	°C
VDD	3.0	3.3	3.6	V
VDDHV during routine test		20		V
VDDHV during normal operation	3.0	3.3	3.6	V

2.2
Absolute Maximum Ratings (Non-Operating)

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability (eq. hot carrier degradation).

Table 2: Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Unit	
DC supply voltage	VDD	-0.3	7.0	V	
DC supply voltage	VDDHV	-0.3	22	V	
Input pin voltage	V_in	-0.3	VDD+0.3	V	
Input current on any pin	I_in	-100	100	mA	Norm: JEDEC78
Storage Temperature	T_strg	-55	125	°C	
Humidity		5	85	%	Non-condensing
Electrostatic discharge	ESD	+/-2		kV	Norm: MIL 883 E method 3015
Soldering Conditions	T_lead				Norm: IEC 61760-1

2.3
Magnetic Specifications

As the chip has no memory for magnetic compensation values it is not magnetically trimmed during the final test, so the raw measurements have huge tolerances.

As described in chapter 6.6 the integrated test circuits can be used to measure the magnetic trim values on module level. With this information and the signal processing described in chapter 6.5 accurate measurements can be done.

Both magnetic specifications for raw values and for on chip calibrated and postprocessed values are given in the following tables.

The min., typ. and max. values are based on a small number of samples from one engineering lot, measured with 3.3 V supply, offset centring regulation settled, OCToggle set to low. Unless otherwise noted 25°C. Drift values are with respect to 25°C. 1σ values are measured while 5σ values are calculated.

Table 3: Magnetic Specifications: Basic configuration with signal processing on microcontroller and on chip magnetic trimming.

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-88		88	mT	-40°C … 125°C 5σ value
		-131		131	mT	5σ value
Magnetic field range Z	BmaxZ	-131		131	mT	-40°C … 125°C 5σ value
		-172		172	mT	5σ value
Magnetic sensitivity XY	SXY	99.7	100.0	100.4	LSB/mT	1σ = 0.173
Magnetic sensitivity Z	SZ	99.8	100.0	100.3	LSB/mT	1σ = 0.136
Magnetic resolution XY			10.0		µT/LSB	
Magnetic resolution Z			10.0		µT/LSB	
Sensitivity drift X, Y		-0.8	0.0	0.8	%	-40°C … 125°C 1σ = 0.43
Sensitivity drift Z		-0.9	0.0	1.1	%	-40°C … 125°C 1σ = 0.55
Sensitivity matching X/Y		99.5	100	100.4	%	-40°C … 125°C 1σ = 0.17
Sensitivity matching XorY/Z		99.7	100	100.3	%	1σ = 0.12
Sensitivity matching drift XorY/Z		-0.6		1.0		-40°C … 125°C
Orthogonality X/Y		89.6	90.1	90.6	°	1σ = 0.26
Orthogonality Z2X or Z2Y		89.6	89.9	90.2	°	1σ = 0.13
Magnetic offset XY	BoffsXY	0.0	0.0	0.0	mT	(1)
Magnetic offset Z	BoffsZ	0.0	0.0	0.0	mT	(1)
Magnetic offset drift XY		-0.38	0.0	0.29	mT	-40°C … 125°C 1σ = 0.27
Magnetic offset drift Z		-0.09	0.0	0.01	mT	-40°C … 125°C 1σ = 0.02
1σ Noise XY			11.6		µT	
1σ Noise Z			9.9		µT	

Basic configuration: GainXY =128, GainZ = 64, UD = 2.6 V.
(1) After offset adjustment. Take care of the geomagnetic field!

Table 4: Magnetic Specifications: Raw Values with basic configuration

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-88		88	mT	-40°C … 125°C 5σ value
		-131		131	mT	5σ value
Magnetic field range Z	BmaxZ	-131		131	mT	-40°C … 125°C 5σ value
		-172		172	mT	5σ value
Magnetic sensitivity XY	SXY	95.4	97.4	100.5	LSB/mT	1σ = 1.6
Magnetic sensitivity Z	SZ	90.9	92.8	94.4	LSB/mT	1σ = 1.4
Magnetic resolution XY			10.27		µT/LSB	
Magnetic resolution Z			10.78		µT/LSB	
Sensitivity drift XY		-39.8		44.9	%	-40°C … 125°C
Sensitivity drift Z		-37.7		40.2	%	-40°C … 125°C
Sensitivity matching X/Y		99.88	100.07	100.28	%	-40°C … 125°C 1σ = 0.09
Sensitivity matching XorY/Z		51.7	52.2	53.2	%	1σ = 0.5
Sensitivity matching drift XorY/Z		-4.3		2.8	%	
Orthogonality X/Y		89.6	90.1	90.6	°	1σ = 0.29
Orthogonality Z/X Z/Y		90.5	92.0	93.0	%	1σ = 0.71
Magnetic offset XY	BoffsXY	-5.2	-0.5	3.7	mT	1σ = 3.05
Magnetic offset Z	BoffsZ	-0.17	-0.0	0.14	mT	1σ = 0.09
Magnetic offset drift XY		-1.60	0.02	1.95	mT	-40°C … 125°C 1σ = 1.09
Magnetic offset drift Z		-0.07	0.00	0.06	mT	-40°C … 125°C 1σ = 0.03
1σ Noise XY			11.6		µT	
1σ Noise Z			9.9		µT	

Table 5: Magnetic Specifications: Small measurement range, raw values

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-9.1		9.1	mT	-40°C … 125°C 5σ value
		-17.7		17.7	mT	5σ value
Magnetic field range Z	BmaxZ	-11.2		11.2	mT	-40°C … 125°C 5σ value
		-14.7		14.7	mT	5σ value
Magnetic sensitivity XY	SXY	193.2		620	LSB/mT	-40°C … 125°C 5σ value
		321.0	377.8	434.5	LSB/mT	5σ value
Magnetic sensitivity Z	SZ	358.2		1011.5	LSB/mT	-40°C … 125°C 5σ value
		543.5	659.5	775.5	LSB/mT	5σ value

Small measurement range configuration: GainXY = 512, Gain Z = 512, UD = 2.6 V

Table 6: Magnetic Specifications: High measurement range, raw values

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Magnetic field range XY	BmaxXY	-1.76		1.76	T	-40°C … 125°C 5σ value
		-2.50		2.50	T	5σ value
Magnetic field range Z	BmaxZ	-2.19		2.19	T	--40°C … 125°C 5σ value
		-2.87		2.87	T	5σ value
Magnetic sensitivity XY	SXY	3.02		9.79	LSB/mT	-40°C … 125°C 5σ value
		5.02	5.90	6.79	LSB/mT	5σ value
Magnetic sensitivity Z	SZ	2.80		7.90	LSB/mT	-40°C … 125°C 5σ value
		4.24	5.15	6.06	LSB/mT	5σ value

High measurement range configuration: GainXY = 64, GainZ = 32, UD = 0.325 V

2.4
Current Consumption

Table 7: Current Consumption

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
IDD during measurements	IDD_{meas}		11.0	15.0	mA	(1, 2, 3)
IDD all analog blocks PD	IDD_{reset}		0.25	0.5	mA	(1, 2)
IDD analog PD, clk off	IDD_{PD}		1	20	µA	(1, 2)

(1) Output currents in I/O pins are not included.
(2) Values are DC mean currents.
(3) Low IDD version available on request

3
Package and Circuit Connection

3.1
Package and Dimension

2.5 x 2.5 x 0.6 mm WLCSP with 0.5 mm ball pitch.

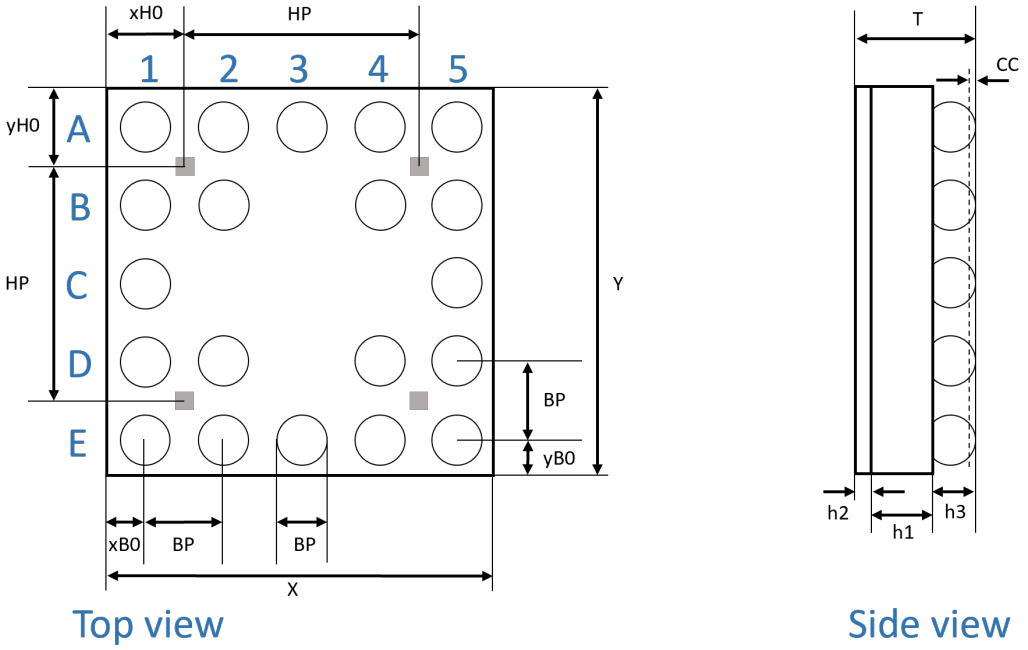

Figure 2: Package Drawing

Table 8: Package Dimensions

Parameter	Symbol	Value	Unit	Note
Hall Sensor Pitch	HP	1500	µm	
Hall Sensor to chip edge	xH0, yH0	507.5	µm	
Chip length	X	2515 ± 20	µm	
Chip width	Y	2515 ± 20	µm	
Chip thickness	T	600±30	µm	
Distance chip border to bumps	xB0, yB0	257.5	µm	
Bump pitch	BP	500	µm	
Wafer thickness	h1	346±15	µm	
Backside Laminate	h2	22±5	µm	
Bump height	h3	232±23	µm	
Solder Ball Coplanarity	CC	40	µm	
Bump diameter	BD	329±20	µm	

Table 9: Pads and pad positions

Pad	Name	Pad position		Protection to
		X	Y	
A3	VDD	1410.00	2266.00	VSS
A2	VSS	1560.00	2266.00	VDD
E4	VDDHV	897.65	176.95	VSSHV
E3	VSSHV	1162.55	176.95	VDDHV
A1	LOCK_N	2266.00	2248.80	VDD/VSS
E1	RESET_N	2266.00	221.20	VDD/VSS
A4	READY	204.00	2040.60	VDD/VSS
A5	MISO	204.00	2248.80	VDD/VSS
B5	MOSI	204.00	1832.40	VDD/VSS
E5	CLK	204.00	221.20	VDD/VSS
C5	SCK	204.00	429.40	VDD/VSS
B2	SCE	2266.00	2040.60	VDD/VSS
E2	TESTM	2266.00	429.40	VDD/VSS
D1	CS_N	2266.00	691.90	VDD/VSS
D5	CSO_N	204.00	637.60	VDD/VSS
B1	TEST	2266.00	1883.30	VDD/VSS

Reference position for x- and y- positions is the lower left chip edge.

The chip size is 2470µm x 2470µm between the scribe outer edges.

Table 10: PCB land pad diameter recommendation

Description	Value	Unit	Note
Non-soldermask defined (NSMD)	270	µm	
Soldermask defined (SMD)	300	µm	

3.2 Pins

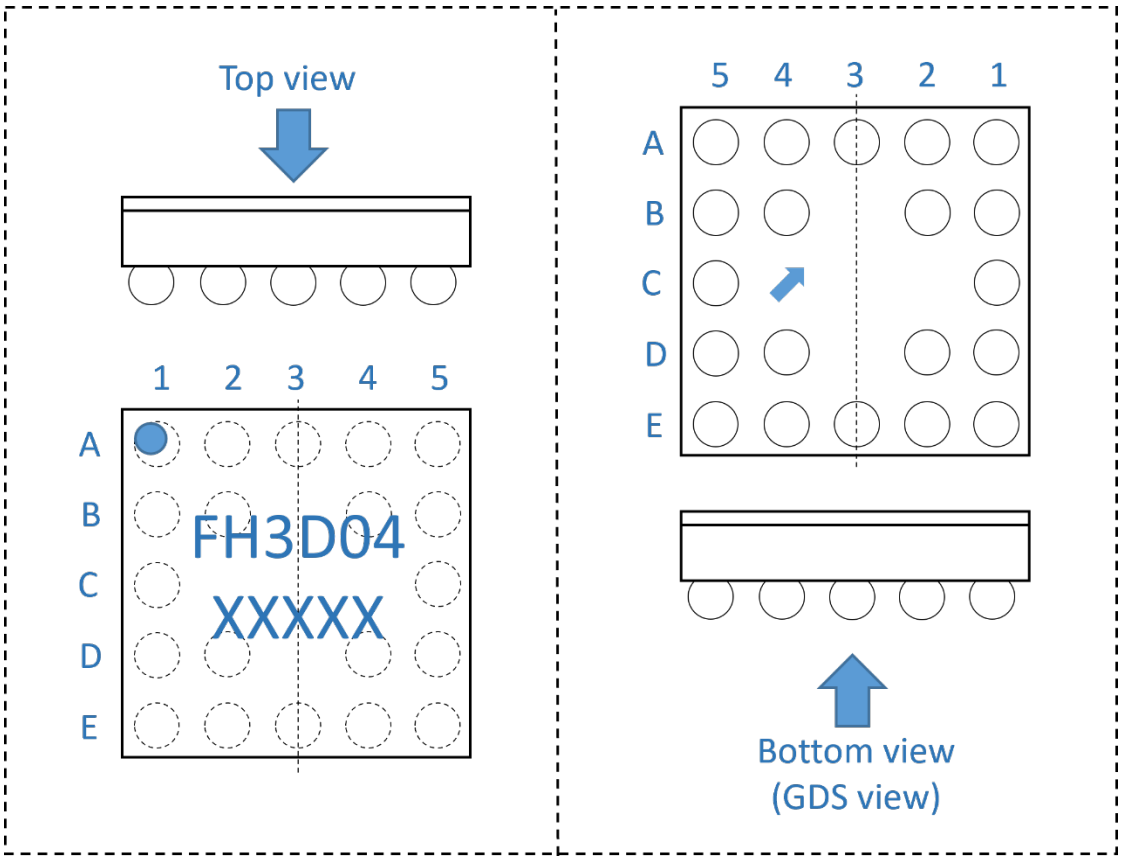

Figure 3: Top and bottom view WLCSP

LOCK_N A1	VSS A2	VDD A3	READY A4	MISO A5
TEST B1	SCE B2		PIN2.NC B4	MOSI B5
PIN1.NC C1				SCK C5
CS_N D1	PIN3.NC D2		PIN4.NC D4	CSO_N D5
RESET_N E1	TEST_M E2	VSSHV E3	VDDHV E4	CLK E5

Figure 4: Top view pinout

Table 11: Pin description

Pin	Name	Pad	Description
A1	LOCK_N	Digital In	Lock, must be connected to VSS
A2	VSS	Supply	Ground (0 V)
A3	VDD	Supply	Supply voltage 3.3 V
A4	READY	Digital Out	Measurement ready signal
A5	MISO	Digital Out	Master in / Slave out (SPI output)
B1	TEST	Analog Out	Test pin
B2	SCE	Digital In	Scan test enable, must be connected to VSS
B5	MOSI	Digital In	Master out Slave in (SPI input)
C5	SCK	Digital In	SPI Interface clock
D1	CS_N	Digital In	Chip Select (low-active)
D5	CSO_N	Digital Out	Chip Select Output (low-active), available on customer request
E1	RESET_N	Digital In	Reset
E2	TESTM	Digital In	Test Mode, must be connected to VSS
E3	VSSHV	Supply	Ground (0 V)
E4	VDDHV	Supply	Supply voltage (3.3 V or 20 V for routine tests)
E5	CLK	Digital In	System clock (8 MHz)

The digital input pins have Schmitt-trigger functionality. The outputs are slew rate controlled CMOS drivers. The corresponding levels are shown in this table and are valid for a junction temperature range of –40 …125°C.

Table 12: Pin input and output levels

Name	Min.	Max.	Unit	Comment
Input negative going threshold	1.12	1.27	V	VDD=3.0V
Input negative going threshold	1.42	1.52	V	VDD=3.6V
Input positive going threshold	1.77	1.87	V	VDD=3.0V
Input positive going threshold	2.07	2.23	V	VDD=3.6V
Output low level	0	0.4	V	8mA load (MISO 16mA)
Output high level	2.5	VDD	V	8mA load (MISO 16mA)

CS_N as low active chip select signal activates receiving and sending of interface data. If only a single chip is used, CS_N can remain ‘low’. All interface data is synchronized internally and transferred after 16 SCK cycles.

The system clock CLK only toggles the state machine and ADC. It can be run at a maximum frequency of 8 MHz.

3.3
Electrical Connection

The sensor chip must be connected to a supply of 3.3 V via its VDD and VSS pins.

The integrated coils may be connected to 3.3 V or up to 20 V depending on the application. If the integrated coils should be used to measure the sensitivity during the final module test in a short time, VDDHV should be connected to 20 V. If the integrated coils should be used to monitor the sensors functionality the integrated coils can be connected to 3.3 V. All unused input pins should be connected to VSS to guarantee proper function. Decoupling capacitors between VDD and VSS as well as between VHHDV and VSSHV close to the sensor chip are strongly recommended. For communication of a single sensor with a microcontroller, all four SPI signals CS_N, SCK, MOSI and MISO have to be connected. After power up, a proper reset cycle of the sensor chip has to be executed. Pin READY can be used to detect a finished measurement.

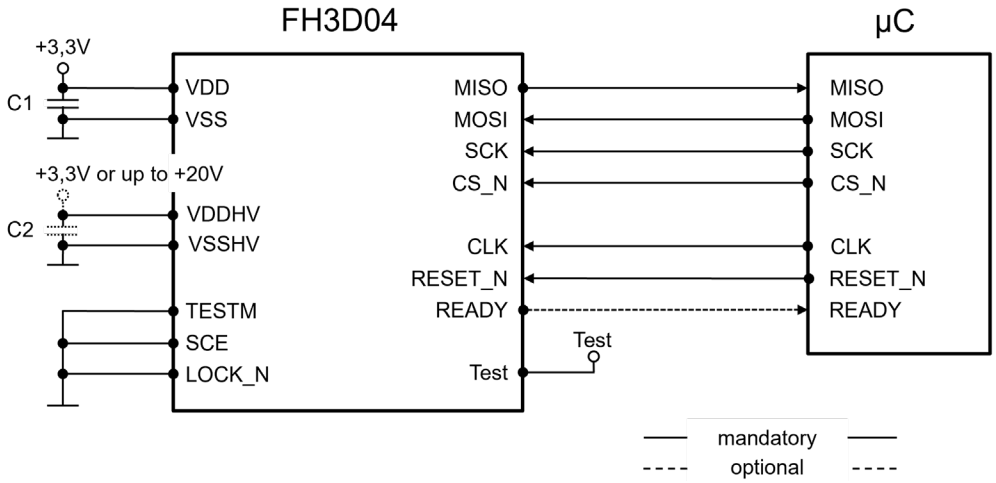

Figure 5: Typical electrical connection

Recommended additional components:
C1: Non-magnetic capacitor near pins (100 nF)
Optional components:
C2: Non-magnetic capacitor near pins (100 nF)

Please note:
It is strongly recommended to use a PCB with wide bandwidth, low impedance supply layer system and impedance controlled digital signal lines with matching series resistors to the hardware setup. A stable supply and clean signals are mandatory for low sensor noise and faultless communication at high SPI frequency.

4
SPI Communication

4.1
Communication Interface

The serial interface samples the information at MOSI with the rising edge of SCK.
The output bits at MISO are updated with every falling SCK edge. MISO is only activated if CS_N is low. Otherwise the output is hi-Z. This allows for parallel operation of multiple ICs.
Two different access modes are possible. A 16 bit word can be written to a certain address or a 16 bit word can be read. The MSB of the address word (A<15>) decides about reading or writing the data.

A<15> = 0 (read measurement data / RAM)
A<15> = 1 (write parameter / RAM)

Writing:
For writing a word into a register the appropriate address and the write/read bit must be written to the interface. The interface counter counts the SCK cycles and detects the end of the address word and the beginning and end of the data word. Therefore the chip select (CS_N) can be set to 'low' and does not need to be controlled.
During the write access the current data in the addressed register is written to MISO. Using this, the interface register behaves like a 32-bit shift register. The chip select does not affect the register but controls the transfer of data only.

Reading:
For reading a register the address with A<15> = 0 is written to the interface. After 16 SCK cycles the actual reading starts.
During clocking out the data from a register at MISO, the bits at MOSI are interpreted as new R/W command and address.

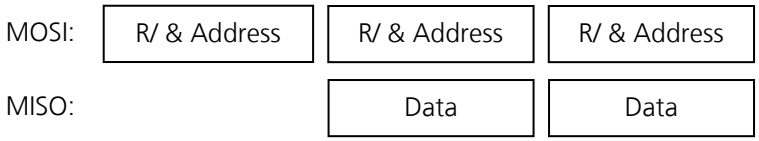

Figure 6: Reading mode

Failure detection:
For detection of communication errors, the current value of a register can be read back at the same time as new data is written to it.

During a write access first the address is transmitted. After the address is written, the interface can read the content of this register and prepare for read back. During writing the new data and finalizing the transmission, the old register content is available at the MISO pin. The controller can verify the old register content.

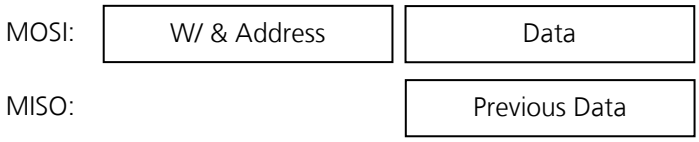

Figure 7: Writing mode

With this function it is possible to check the connection between ASIC and controller as well as the content of the concerning register.
After a write command transfer is complete, the complete transfer data is present at MISO during the next transfer phase. The correct communication can be verified here.

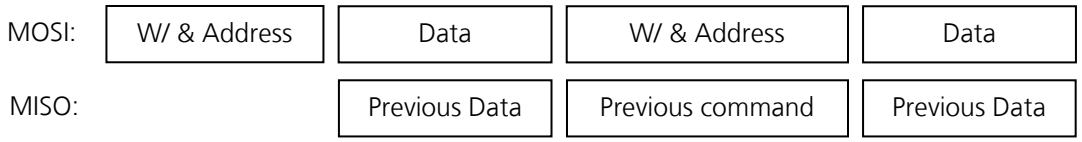

Figure 8: Command verification

SPI synchronization:

While usually CS_N can stay active (low) over many periods of word transfers, it may happen in harsh environments, that spikes on the SCK signal disturb internal synchronization of the slave's interface to the master's one. In such cases the CS_N signal can be set to high in order to reset the internal SCK counter. Thus, synchronization of master and slave can be restored.

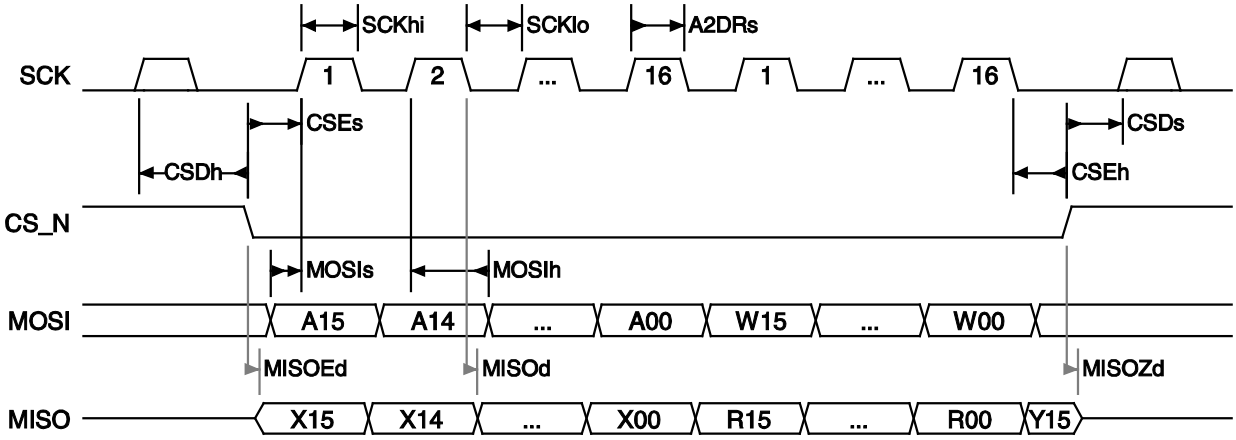

Figure 9: SPI timing

Table 13: SPI timing values

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
External CLK frequency	f_{CLK}	7.950	8	8.05	MHz	
External CLK pulswidth HI	t_{CLKhi}	62	62.5	63	ns	
External CLK pulswidth LO	t_{CLKlo}	62	62.5	63	ns	
External CLK duty cycle	D_{CLK}	49	50	51	%	
SCK frequency Standard registers	f_{SCK}	0		16	MHz	(1)
SCK pulswidth HI	t_{SCKhi}	30	31.25		ns	
SCK pulswidth LO	t_{SCKlo}	30			ns	
CS_N enable setup time before SCK	t_{CSEs}	10			ns	
CS_N enable hold time after SCK	t_{CSEh}	10			ns	
CS_N disable setup time before SCK	t_{CSDs}	10			ns	
CS_N disable hold time after SCK	t_{CSDh}	10			ns	
MOSI setup time before SCK	t_{MOSIs}	10			ns	
MOSI hold time after SCK	t_{MOSIh}	10			ns	
MISO delay after SCK	t_{MISOd}			10	ns	
MISO enable delay after CS_N	t_{MISOEd}			20	ns	
MISO high Z delay after CS_N	t_{MISOZd}			20	ns	
Output edge rise time	t_{Or}		3	8	ns	
Output edge fall time	t_{Of}		3	8	ns	

Typical values are given for 25°C. Output load of MISO is 100 pF, other outputs 25 pF.
(1) must not exceed $8 \cdot f_{CLK}$

4.2
Multiple CS_N Parallel Operation

FH3D04 is optimized for being stitched to lines or areas with 1.5 mm pixel distance. The simplest way to communicate with several ICs for combined operation is to use separate CS_N wires for every device. Communication with a device is only possible while CS_N is low. Then the output MISO is active, otherwise it is high impedance.

It then is important that only one CS_N signal is active at a time to avoid shorts and thus distortions on the MISO signal.

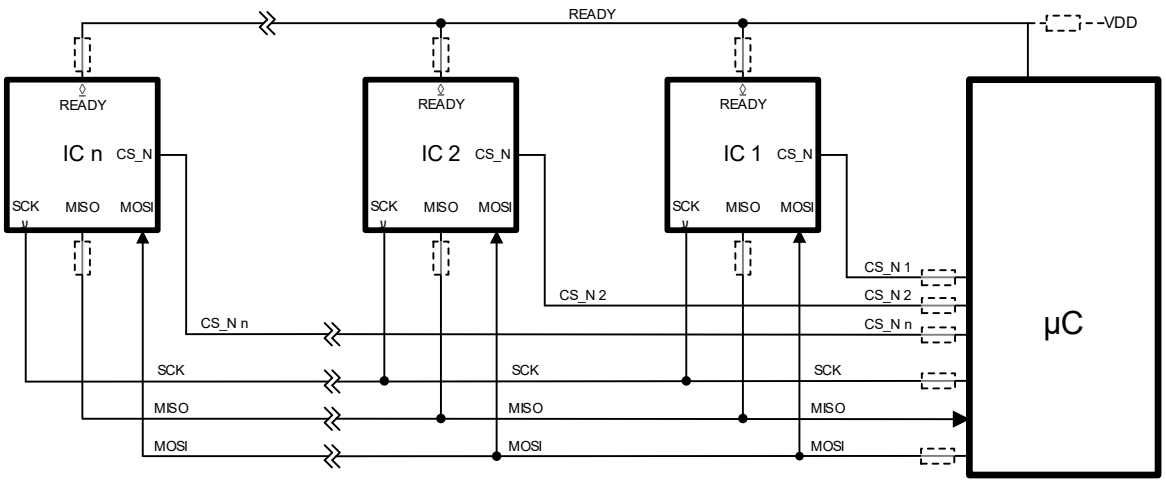

Figure 10: Example for configuration with several FH3D04 devices and one master controller in chip select mode.

In combination with an external pull up resistor to the supply voltage (VDD) the READY output can be configured to act as an open drain output such that a wired and combination of all READY signals clearly indicates the end of every measurement in all devices.

If the routings between the devices are long, a series resistor close to the driving output is recommended to avoid (or at least suppress) distortions due to reflections in the lines at the receiving devices (see dashed resistors).

4.3
Adressed Parallel Operation

In parallel operation Daisy Chain is only available on customer request, but addressing is available and ensures comfortable selection of single FH3D04 without CS_N low/high operations after initialization (e.g. for DMA driven data transfers).

During initialization to a via CS_N low selected FH3D04 an address can be assigned by using SPI address 0x009. If all parallel FH3D04 have an address all CS_N can stay low and a device can be addressed and activated by using SPI address 0x00A. The register content is described in the following tables.

Table 14: Register 0x009 bit assignment

Bitpos.	Signal	Meaning
15-8	OwnAddrGrp	Set own group address
7-0	OwnAddr	Set own address

Table 15: Register 0x00A bit assignment

Bitpos.	Signal	Meaning
15-8	AddrGrp	Chip select with own group address
7-0	Addr	Chip select with own address

For operating a system in such a configuration it is necessary to assign a unique OwnAddr to every device before it can be addressed. The following sections describe the necessary procedures.

Distributing OwnAddr Values

Distributing the addresses to several devices on the same SPI is possible by selecting the single device via CS_N low. After setting an OwnAddr ≠ 0 the active device will be deactivated.

Addressing

Holding all available CS_Ns low and writing an address into register 0x00A via SPI activates only the chip whose OwnAddr<7:0> is identical to the written Addr<7:0>. CS_N must be low during the write command. ICs whose OwnAddr is not identical are deactivated. In this way it is possible to switch from one already addressed chip to another by a single write command to address 0x00A.

5
Register Map

Following tables show all available registers for communication with the sensor via SIP.
After a reset the electrical trim values have to be read out of OTP via registers 0x050 and 0x051 and configuration registers 0x002 to 0x040 have to be written once. Measurements can be started using register 0x001. The measured values can be read from register 0x100, while 0x102 contains status bits. A read operation from register 0x100 deletes the ready bit.

Table 16: Register 0x001 content

Bitpos.	Signal	Width	Meaning
15-13	AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	TempSel	1	Temperature Select
11-10	PixelSel<1:0>	2	Pixel Select 0: upper left 3D Hall sensor, 1: upper right 3D Hall sensor 2: lower right 3D Hall sensor, 3: lower left 3D Hall sensor
9-8	SensSel<1:0>	2	Sensor Select <1:0> : Sensor: 0 = X, 1 = Y, 2 = Z, 3 = Hall sensor off
7-1	DecLen<7:1>	7	Decimation Length lower bits DecLen<0> is always 0 If DecLen<10:1> is 0 DecLen = 1
0	DecEn	1	Decimation Enable

To start a measurement with basic configuration using register 0x001 write via SPI transfer:
8001h – ??01h Pixel ?, Sensor ?, Gain ?, DecLen<10:8> +0

Table 17: Register 0x002 content

Bitpos.	Signal	Width	Meaning
15-13	AmpComp<2:0>	3	Amplifier Compensation 7 = auto compensation
12	Fast2P	1	Fast two phase SC
11	SMUXChopInv	1	Sensor MUX Chopper Invert
10-8	DecLen<10:8>	3	Decimation Length upper bits If DecLen<10:1> is 0 DecLen = 1
7-0	DecWait<7:0>	8	Decimation Wait, has to be at least 3

For basic configuration of register 0x002 write via SPI transfer:
8002h – E250h AmpComp: 7; DecLen: 2*256+(DecLen<7:1>*2); DecWait: 80

Table 18: Register 0x003 content

Bitpos.	Signal	Width	Meaning
15-13	SRegDVal<2:0>	3	Sensor Regulator Difference Value 0 = 0.325V, 1 = 0.65V, 2 = 1.3V 3 = 2.0V, 5 = 2.6V, 6 = 2.8V
12-10	SRegNVal<2:0>	3	Sensor Regulator Negative Value 0 = 0.2V, 2 = 0.5V, 3 = 0.65V 5 = 0.95V, 6 = 1.1V
9-6	ECCSel<3:0>	4	„Excitation Current Coil Select“ Activates the calibration coil. 0: coils off 1: P2 XY 2: P2 Q 3: P2 Z + P1 H 4: P2 H + P1 Z 5: P1 Q 6: P1 XY 7: P3 XY 8: P3 Q 9: P3 Z + P0 H 10: P3 H + P0 Z 11: P0 Q 12: P0 XY
5-3	ECVal<2:0>	3	Excitation Current Value
2	ECSign	1	Excitation Current Sign
1-0	Phase<1:0>	2	Phase

For basic configuration of register 0x003 write via SPI transfer:
8003h – A000h SRegDVal:5 = 2.6 V; SRegNVal:0 = 0.2 V

Table 19: Register 0x004 content

Bitpos.	Signal	Width	Meaning
15	Reserved	1	Reserved set to zero
14	ModOpM	1	Modulator Operating Mode
13	ECEnHV	1	Excitation Current Enable High Voltage 0: 0.2mA per Digit (EC_Val+1) 1: 1.4mA per Digit (EC_Val+1)
12-9	Auto4P<3:0>	4	Auto4P
8	OCSign	1	Offset Centering Sign
7-6	OCMode<1:0>	2	Offset Centering Mode Typical: 0b10
5	OCAuto	1	Auto Centering
4	OCIRefR	1	Offset Centering Current Reference Resistor
3	OCToggle	1	Offset Centering Toggle
2-0	OCGain<2:0>	3	Offset Centering Gain

For basic configuration of register 0x004 write via SPI transfer:
8004h – 0AA9h Auto4P:0101b; OCMode:10b; OCAuto; OCToggle; OCGain: 001b

Table 20 Register 0x005 content

Bitpos.	Signal	Width	Meaning
15-6	Reserved	10	Reserved set to zero
5	Rng2Reg100	1	Write the range warning bit in register 100
4	SeqNr2Reg100	1	Write the sequencer number in register 100
3	Parity2Reg100	1	Write the parity bit in register 100
2-1	RM<1:0>	2	Ready Mode
0	RVR1	1	Read Value Register 1

For basic configuration of register 0x005 write via SPI transfer:
8004h – 0002h RM: 1

Table 21: Register 0x006 content

Bitpos.	Signal	Width	Meaning
15-11	Reserved	5	Reserved set to zero
10	OC_PO	1	Offset Centering PO
9	ModRefBuf_PO	1	Modulator Reference Buffer Power On
8	Buf_PO	1	Buffer Power On
7	EC_PO	1	Excitation Current Power On
6	Bias_PO	1	Bias Power On
5	Mod_PO	1	Modulator Power On
4	Amp_PO	1	Amplifier Power On
3	SRegN_PO	1	Sensor Regulator N Power On
2	SRegD_PO	1	Sensor Regulator D Power On
1	SMUXPowerEn	1	Sensor Modulator Power Enable
0	SMUXSigEn	1	Sensor Mux Signal Enable

For basic configuration of register 0x004 write via SPI transfer:
8006h – 077Fh all PO except EC_PO; SMUXPowEn;

Table 22: Register 0x007 content

Bitpos.	Signal	Width	Meaning
15-0	Reserved	16	Reserved, has to be 0

For basic configuration of register 0x007 no action is needed.

Table 23: Register 0x008 content

Bitpos.	Signal	Width	Meaning
15	SConstI_PO	1	"Sensor Constant Current PowerOn"
14	SIMeasEn	1	"Sensor Current Measurement Enable" 0: Temperature measurement 1: Current measurement
13	SIMeas_PO	1	"Sensor Current Measurement Power On" Switch on the current measurement.
12-6	IbBoost<6:0>	7	I Bias Boost <6> IbBoostEC <5> IbBoostAmp <4> IbBoostBuf <3> IbBoostSupReg <2> IbBoostMod <1> IbBoostRefBuf <0> IbBoostOC
5-4	ICTEn<1:0>	2	In-Circuit-TestEnable <1> Disconnect Test4/3 from GND and connect is to the pads. <0> Disconnect Test2/1 from GND and connect is to the pads.
3	ICTUP	1	In-Circuit-Test UP Switch positive sensor supply voltage to *TEST*. *ICTEn<0> has to be set.*
2	ICTUN	1	In-Circuit-Test UN Switch negative sensor supply voltage to *TEST*. *ICTEn<0> has to be set.*
1	ICTIb	1	In-Circuit-Test Ib Switch 10uA reference current to *TEST*. *ICTEn<0> has to be set.*
0	ICTURef	1	In-Circuit-Test URef Switch bandgap reference voltage to *TEST*. *ICTEn<0> has to be set.*

For basic configuration of register 0x008 no action is needed.

Table 24: Register 0x009 content

Bitpos.	Signal	Width	Meaning
15-8	OwnAddrGrp	8	Set own group address
7-0	OwnAddr	8	Set own address

For basic configuration of register 0x009 no action is needed.

Table 25: Register 0x00A content

Bitpos.	Signal	Width	Meaning
15-8	AddrGrp	8	Chip select with own group address
7-0	Addr	8	Chip select with own address

For basic configuration of register 0x00A no action is needed.

Table 26: Register 0x00B content

Bitpos.	Signal	Width	Meaning
15-4	Reserved	12	Reserved set to zero
3-0	BgndTempMeas<3:0>	4	Background temperature measurement

For basic configuration of register 0x00B no action is needed.

Table 27: Register 0x010 content

Bitpos.	Signal	Width	Meaning
15-8	Reserved	8	Reserved set to zero
7-0	OCVal0<7:0>	8	Offset Centering Value 0

For basic configuration of register 0x010 no action is needed.

Table 28: Register 0x02F content

Bitpos.	Signal	Width	Meaning
15-2	Reserved	14	Reserved set to zero
1	Reserved	1	Reserved set to zero
0	SeqEn	1	Sequencer enable

For basic configuration of register 0x02F no action is needed.

Table 29: Register 0x030 content

Bitpos.	Signal	Width	Meaning
15-13	Seq0AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	Seq0TempSel	1	Temperature Select
11-10	Seq0PixelSel<1:0>	2	Pixel Select 0: upper left 3D Hall sensor, 1: upper right 3D Hall sensor 2: lower right 3D Hall sensor, 3: lower left 3D Hall sensor
9-8	Seq0SensSel<1:0>	2	Sensor Select <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z, 3 = all sensors off
7-1	Seq0DecLen<7:1>	7	Decimation Length <0> is always 0 If DecLen<10:1> is 0 DecLen = 1
0	Seq0DecEn	1	Decimation Enable

For basic configuration of register 0x030 no action is needed.

Table 30: Register 0x031 content

Bitpos.	Signal	Width	Meaning
15-13	Seq1AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	Seq1TempSel	1	Temperature Select
11-10	Seq1PixelSel<1:0>	2	Pixel Select 0: upper left pixel, 1: upper right pixel 2: lower right pixel, 3: lower left pixel
9-8	Seq1SensSel<1:0>	2	Sensor Select <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z, 3 = all sensors off
7-1	Seq1DecLen<7:1>	7	Decimation Length <0> is always 0 If DecLen<10:1> is 0 DecLen = 1
0	Seq1DecEn	1	Decimation Enable

For basic configuration of register 0x031 no action is needed.

Table 31: Register 0x032 content

Bitpos.	Signal	Width	Meaning
15-13	Seq2AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	Seq2TempSel	1	Temperature Select
11-10	Seq2PixelSel<1:0>	2	Pixel Select 0: upper left 3D Hall sensor, 1: upper right 3D Hall sensor 2: lower right 3D Hall sensor, 3: lower left 3D Hall sensor
9-8	Seq2SensSel<1:0>	2	Sensor Select <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z, 3 = all sensors off
7-1	Seq2DecLen<7:1>	7	Decimation Length <0> is always 0 If DecLen<10:1> is 0 DecLen = 1
0	Seq2DecEn	1	Decimation Enable

For basic configuration of register 0x032 no action is needed.

Table 32: Register 0x033 content

Bitpos.	Signal	Width	Meaning
15-13	Seq3AmpGain<2:0>	3	Amplifier Gain 0=32, 1=64, 2=128, 3=256, 4=512, 5=1024, 6 and 7 is not allowed
12	Seq3TempSel	1	Temperature Select
11-10	Seq3PixelSel<1:0>	2	Pixel Select 0: upper left 3D Hall sensor, 1: upper right 3D Hall sensor 2: lower right 3D Hall sensor, 3: lower left 3D Hall sensor
9-8	Seq3SensSel<1:0>	2	Sensor Select <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z, 3 = all sensors off
7-1	Seq3DecLen<7:1>	7	Decimation Length <0> is always 0 If DecLen<10:1> is 0 DecLen = 1
0	Seq3DecEn	1	Decimation Enable

For basic configuration of register 0x033 no action is needed.

Table 33: Register 0x40 content

Bitpos.	Signal	Width	Meaning
15	Reserved	1	Reserved, set to zero
14-9	BGTrim<5:0>	6	Bandgap Trim
8-4	IBiasTrim<4:0>	5	Trim bits for IBias generation
3-0	SRegTrim<3:0>	4	Trim bits for sensor regulator

For basic configuration of register 0x040 with typical electrical trim values write via SPI transfer:
8040h – 4058h BGTrim=32; IBiasTrim=5; SRegTrim=8
Attention: Electrical trim values are device dependent and have to be read from OTP at startup.

Table 34: Register 0x050 content

Bitpos.	Signal	Width	Meaning
15-8	Reserved	8	Reserved set to zero
7-0	FuseAddr<7:0>	8	Fuse Address

For basic configuration of register 0x050 no action is needed.

Table 35: Register 0x051 content

Bitpos.	Signal	Width	Meaning
15-8	Reserved	8	Reserved set to zero
7-0	FuseData<7:0>	8	Fuse Data

For basic configuration of register 0x051 no action is needed.

Table 36: Register 0x100 content

Bitpos.	Signal	Width	Meaning
15	DecVal<15> RngWarn SeqNr<1> Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
14	DecVal<14> SeqNr<1> SeqNr<0> Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
13	DecVal<13> SeqNr<0> Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
12	DecVal<12> Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
11-0	DecVal<11:0>	12	Decimation Value

Table 37: Register 0x102 content

Bitpos.	Signal	Width	Meaning
15	Ready	1	Ready
14	HistWarn	1	Histogram Warning
13	RngWarn	1	Range Warning
12-11	Reserved	2	Reserved set to zero
10-9	SeqNr<1:0>	2	Sequencer number
8-4	FC<4:0>	5	Field Component <4>: Temperature <3:2>: Pixel <1:0>: Sensor: 0 = X, 1 = Y, 2 = Z,
3-1	Reserved	3	Reserved set to zero
0	DecVal<16>	1	Decimation Value MSB; only relevant if measurement result width is 17 Bit

Table 38: Register 0x103 content

Bitpos.	Signal	Width	Meaning
15-0	{Reserved<7:0>, OCVal<7:0>} or HistVal<15:0>	16	Offset Centering Value if one of the Auto4P Bits is set otherwise Histogram in single phase measurements

Table 39: Register 0x104 content

Bitpos.	Signal	Width	Meaning
15-0	TempVal<15:0>	16	Temperature Value of the background temperature measurement

Table 40: Register 0x130 content

Bitpos.	Signal	Width	Meaning
15	Seq0DecVal<15> Seq0RngWarn Seq0SeqNr<1> Seq0Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
14	Seq0DecVal<14> Seq0SeqNr<1> Seq0SeqNr<0> Seq0Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
13	Seq0DecVal<13> Seq0SeqNr<0> Seq0Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
12	Seq0DecVal<12> Seq0Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
11-0	Seq0DecVal<11:0>	12	Decimation Value

Table 41: Register 0x131 content

Bitpos.	Signal	Width	Meaning
15	Seq1DecVal<15> Seq1RngWarn Seq1SeqNr<1> Seq1Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
14	Seq1DecVal<14> Seq1SeqNr<1> Seq1SeqNr<0> Seq1Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
13	Seq1DecVal<13> Seq1SeqNr<0> Seq1Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
12	Seq1DecVal<12> Seq1Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
11-0	Seq1DecVal<11:0>	12	Decimation Value

Table 42: Register 0x132 content

Bitpos.	Signal	Width	Meaning
15	Seq2DecVal<15> Seq2RngWarn Seq2SeqNr<1> Seq2Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
14	Seq2DecVal<14> Seq2SeqNr<1> Seq2SeqNr<0> Seq2Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
13	Seq2DecVal<13> Seq2SeqNr<0> Seq2Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
12	Seq2DecVal<12> Seq2Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
11-0	Seq2DecVal<11:0>	12	Decimation Value

Table 43: Register 0x0133 content

Bitpos.	Signal	Width	Meaning
15	Seq3DecVal<15> Seq3RngWarn Seq3SeqNr<1> Seq3Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
14	Seq3DecVal<14> Seq3SeqNr<1> Seq3SeqNr<0> Seq3Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
13	Seq3DecVal<13> Seq3SeqNr<0> Seq3Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
12	Seq3DecVal<12> Seq3Parity	1	Depending on Rng2Reg100 SeqNr2Reg100 Parity2Reg100
11-0	Seq3DecVal<11:0>	12	Decimation Value

6
Application Notes

In this chapter a step-by-step instruction is given to use the sensor in a proper way.
With the basic configuration (chapter. 6.1) first measurements can be done for bring-up.
Using the described signal postprocessing (chapter. 6.5) and the determination of magnetic trim values (Chap. 6.6) measurements over temperature with a high accuracy can be realized.

6.1
First raw measurements with the basic configuration

A decimation length of 512 leads to a resolution of 15 bit.
The wait length can be equal for all sensors. The typical wait length for this decimation length is 80.
The sensor supply regulator has to be set to UD = 2.6 V.
The gain is different for XY and Z sensors. XY sensors use gain 128, Z sensors use gain 64.

6.1.1
Basic configuration

The basic configuration has to be written once after a sensor reset.
The default trim values for the bandgap reference, bias current and sensor supply regulator are:

- ICT_VREF_TRIM: 6'b100000
- ICT_IBIAS_TRIM: 4'b0101
- ICT_SREG_TRIM: 4'b1000

The device specific values are available in the OTP (please refer to chapter 7.5) and have to be used in application. For a basic configuration please send the following commands:

- **8040h – 4058h**
  - BGTrim 32; IBiasTrim 5; SRegTrim 8
- **8002h – E250h**
  - AmpComp: 7; DecLen: 2*256+(DecLen<7:1>*2); DecWait: 80
- **8003h – A000h**
  - SRegDVal:5 = 2.6 V; SRegNVal:0 = 0.2 V
- **8004h – 0AA9h**
  - Auto4P:0101b; OCMode:10b; OCAuto; OCToggle; OCGain: 001b
- **8005h – 0002h**
  - RM 1
- **8006h – 077Fh**
  - all PO except EC_PO; SMUXPowEn; SMUXSigEn

6.1.2
Measurement of Pixel 0, Sensor X, Gain 128, DecLen 512

- Gain 128 = 2-> 010b
- PixelSel = 00b
- SensSel = X = 00b
- DecLen = 512 = 200h -> DecLen<7:1>=0 -> 0000000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 4001h** Pixel 0, Sensor X, Gain 128, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.1.3
Measurement of Pixel 1, Sensor Z, Gain 64, DecLen 512

- Gain 64 = 1-> 001b
- PixelSel = 1b
- SensSel = Z = 10b
- DecLen = 512 = 200h -> DecLen<7:1>=0 -> 0000000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 2601h** Pixel 1, Sensor Z, Gain 64, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.1.4
Measurement of the Temperature, with preheating of the next Sensor Pixel 0, Sensor X, Gain 128, DecLen 512

For a constant power consumption and a stable sensor temperature the next hall sensor can be activated during the temperature measurement. The gain setting for the next hall sensor has to be used.

- Gain 128 = 2-> 010b
- TempSel = 1b
- PixelSel = 0b
- SensSel = X = 00b
- DecLen = 512 = 200h -> bit 3 to 0 are allways 0 -> 100000b
- DecEn = 1b start measurement

Send the following command to start the measurement:

- **8001h – 5041h** Pixel 0, Sensor X, Gain 128, DecLen 512

Read out measurement by sending the following commands as described in chapter 4.1.

- **0102h – 0100h – 0000h**

6.2 High speed measurement configuration using sequencer

Single hall sensor elements can be measured with up to 80 kHz at 10 Bit resolution. In sequencer mode the measurements are taken continuously. The SPI communication has no influence to the measurement frequency.
For details about sequencer configuration please refer to chapter 7.4.
Another option for communication in high speed configurations is continuous measurement, please refer to chapter 7.3.1.

Basic configuration:

- **8040h – 4058h**
  - BGTrim 32; IBiasTrim 5; SRegTrim 8
- **8002h – F00Ah**
  - AmpComp 7; Fast2P; DecWait 10
- **8003h – A000h**
  - SRegDVal:5 = 2.6 V; SRegNVal:0 = 0.2 V
- **8004h – 0AA9h**
  - Auto4P:0101b; OCMode:10b; OCAuto; OCToggle; OCGain: 001b
- **8005h – 003Ah**
  - Rng2Reg100; SeqNr2Reg100; Parity2Reg100, RM 1
- **8006h – 077Fh**
  - all PO except EC_PO; SMUXPowEn; SMUXSigEn

Sequencer configuration: Z-Sensor Pixel 0, Gain 256, DecLen 34

- **8030h – 6223h**
  - Gain 256; Pixel 0; Sensor Z; DecLen 34, DecEn

Sequencer start:

- **802Fh – 0001h**
  - SeqEn

Measurement value readout: Read data and status at every READY toggle. Alternatively read from register 0x100.

- **0130h – 0000h**
  - Seq0RngWarn, Seq0SeqNr, Seq0Parity, Seq0DecVal

Resolution:

- DecLen: 34, Number of phases: 2, ±7.5 Digit/decimation cycle
  34 * 2 * (+7.5 – (-7,5)) * 2) = 1020→ **10 Bit**

Measurement time / sample rate:

- DecWait: 10; DecLen: 34, Number of phases: 2
  (6 +10 + 34) * 2 = 100 cycles @ 8 MHz system clock
  → measurement time 12.5 µs, sample rate **80 kHz**

6.3 Magnetic resolution

The basic configuration is working in four-phase spinning current scheme with a decimation length of 512. As the ∑Δ-ADC has a resolution of 4 bit and is symmetrical around 0. The maximum ADC value magnitude is 7.5.

The measurement values are in the range of ±15360 which is a resolution of 14.9 bit.

The following picture shows the signal path and its typical parameters.

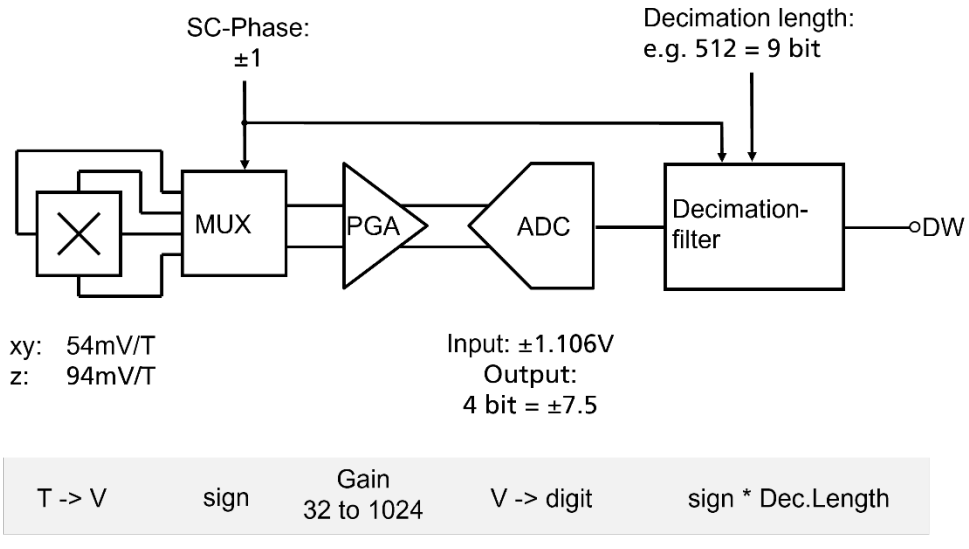

Figure 11: Signal Path

With a differential input of the ADC of ±1.106 V, a 4-bit resolution, a decimation length of 512 a gain of 128 and a 4 phase spinning current scheme the resolution of the ADC can be calculated to:

(2*1.06 V) / 128 / (512 * 15 * 4) = 539.1 nV

With a sensitivity of 54 mV/T for the X and Y sensors the magnetic resolution can be calculated to:

539.1 nV / 54 mV/T = 9.98 µT.

With a gain of 64 and a sensitivity of 94 mV/T the magnetic resolution of the Z sensors is:

(2*1.06 V) / 64 / (512 * 15 * 4) = 1078.3 nV

1078.3 nV / 94 mV/T = 11.47 µT

6.4 Measurement time

In the basic configuration the hall sensors are operated in a four-phase spinning current scheme while the temperature sensor always is operated in a two phase chopper principle.
The pure measurement time can be calculated by:

- (DecLen + DecWait + 6) * **4** * (nr. of hall sensors) + (DecLen+ DecWait + 6) * **2**
- (512 + 80 + 6) * 4 * 3 + (512 + 80 + 6) *2 = 8372
- MHz = 125 ns
- 8372 * 125ns = 1046.5 µs

If the SPI runs at 16MHz the time for communication can be calculated by:

- 16 bit address + 16 bit data = 32 bit
- 16MHz = 62.5 ns
- Per sensor (magnet or temperature) 1 x start + 2 x read
- 32 * 4 * 3 * 62.5 ns = 24 µs

The complete measurement time for all tree hall sensors and the temperature sensor is about 1070.5 µs including all the communication in non-interleaved mode.

6.5 Signal postprocessing

In many applications, the raw senor values can be used without any postprocessing. In this case the parameters described in Table 4 can be used. If the performance described in Table 3 is needed the raw measured digital values have to be converted into magnetic flux density values by using the following signal postprocessing. The necessary parameters can be generated on chip by using the integrated excitation wires as described in chapter 6.6. If higher accuracies are needed the sensitivities and offsets have to be measured by using 3D Helmholtz coils.

6.5.1
Temperature postprocessing

As in constant voltage supplied mode the sensitivity of the Hall sensors is temperature dependent the temperature has to be measured. The necessary temperature postprocessing is shown in Figure 12.

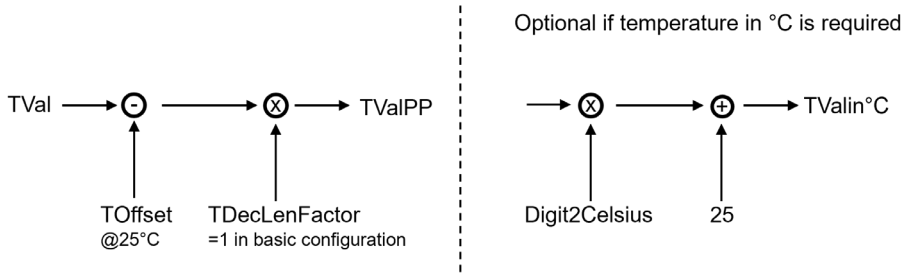

Figure 12: Temperature postprocessing

Using the basic configuration, the temperature value $TVal$ has only to be compensated with the device specific temperature offset $TOffset$ which has to be measured at 25°C.

$$TOffset = TVal(at\ 25°C)$$

This postprocessed temperature value $TValPP$ can then be used for the magnetic postprocessing.

$$TValPP = TVal - TOffset$$

If a different configuration is used the measured temperature value $TVal$ hast to be scaled by the factor $TDecLenFactor$ which can be calculated by:

$$TDecLenFactor = \frac{512}{DecLen}$$

If the temperature in °C is needed $TValPP$ can be converted in °C by the factor $Digit2Celsius$.

$$Digit2Celsius = 0.072484471\,\frac{°C}{Digit}$$

The temperature in °C can be calculated by:

$$TValin°C = TValPP * Digit2Celsius + 25°C$$

6.5.2
Magnetic postprocessing

The necessary magnetic postprocessing is shown in Figure 13.

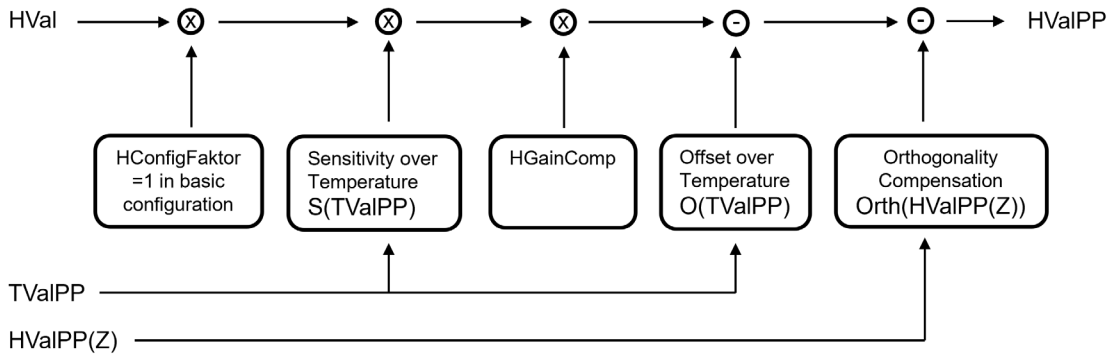

Figure 13: Magnetic postprocessing

Using the basic configuration, the digital hall signal $HVal$ can be converted from Digit to Tesla over temperature using the direction specific typical functions $S_{XY}(\,TValPP)$ or $S_Z(TValPP)$.

$$S_{Typ,XY}(\,TValPP) = 2.4864 \times 10^{-14} \times TValPP^3 + 5.4240 \times 10^{-10} \times TValPP^2 + 4.1604 \times 10^{-6} \times TValPP + 0.010687$$

$$S_{Typ,Z}(TValPP) = 2.6029 \times 10^{-14} \times TValPP^3 + 5.6780 \times 10^{-10} \times TValPP^2 - 4.3553 \times 10^{-6} \times TValPP + 0.011187$$

If different configurations than the basic configurations are used the measured Hall values $HVal$ have to be scaled to the basic configuration parameters (decimation length of 512; gain 128 for XY, gain 64 for Z; sensor supply) by the factor $HConfigFactor$ which can be calculated by:

$$HConfigFactor = \frac{1}{\left(\frac{UsedGain}{BasicGain}\right) \times \left(\frac{UsedDecLen}{BasicDecLen}\right) \times \left(\frac{UsedSupply}{BasicSupply}\right)}$$

For high accuracies as described in Table 3, the device specific production deviations concerning nominal sensitivity, amplifier gains and sensor supply regulator voltages has to be compensated using the factor $HGainComp$ which needs to be calculated for each sensor. Chapter 6.6 describes how this value can be measured.

The magnetic values in Tesla have to be compensated with the device and sensor specific magnetic offsets over temperature $O(TValPP)$. The minimum offset compensation should be done at 25°C as described in chapter 6.6. For higher accuracies the offset temperature coefficient has to be used as described in chapter 6.6.

As the orthogonality errors Z/X and Z/Y can be in the range of several degrees. Depending on accuracy needed in application these orthogonality errors have to be compensated by the coefficient $Orth_{XY}(\mathrm{HV}alPP(Z))$. Chapter 6.6 describes how these factors can be measured on chip.

Using the basic configuration, the postprocessed magnetic field values can be calculated by:

$$HValPP_Z = HVal_Z \times HGainComp \times S_Z(TValPP) - O_Z(TValPP)$$

$$HValPP_{XY} = HVal_{XY} \times HGainComp \times S_{XY}(TValPP) - O_{XY}(TValPP) - Orth_{XY}(HValPP_Z(TValPP))$$

6.6 Determination of magnetic trim values using the integrated excitation coils

The integrated excitation coils can be used to measure the sensors sensitivities, offsets and offset temperature coefficients due to self-heating. If possible choose the maximum excitation current and supply voltage to get low noise measurements and high self-heating effects. Perform this test at room temperature (25°C).

At first the magnetic trimming measurement sequence has to be implemented.
Ensure Excitation Current Power On is set (EC_PO), measure Coil Current (pin VDD_HV) in parallel to measurements.

- Loop over Sensitivity (and CrossSensititivity) coils
  - Loop over used pixels (PixelSel)
    - Loop over used sensor directions (SensSel)
      - Perform measurement on temperature sensor (TempSel=1) and preheat (activate) desired next sensor (PixelSel and SensSel), read decimation value.
      - Set appropriate coil (ECCSel) according to Table 45, current value (ECVal) and ECEnHV according to Table 44 and set ECSign to 1
      - Perform measurement on magnetic field sensor, read decimation value and store it with correct sign according to Table **95**, postfix P
      - Change ECSign to 0.
      - Perform measurement on magnetic field sensor, read decimation value and store it with correct sign according to Table **95** postfix N

Table 44: Excitation coil configuration depending on the available supply voltage.

Supply Voltage	Excitation Current	Mode	Configuration
3.3 V	1.0 mA	LV	ECEnHV = 0; ECVal<2:0> = 100
5 V	1.6 mA	LV	ECEnHV = 0; ECVal<2:0> = 111
9 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010
12 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010
20 V	4.2 mA	HV	ECEnHV = 1; ECVal<2:0> = 010

Table 45: Coil configuration for on-chip calibration

Pixel	SensSel	Coil Setup	ECCSel
0	Z	Sensitivity	ZP0+HP1
0	Y	Sensitivity	XYP0
0	X	Sensitivity	XYP0
1	Z	Sensitivity	ZP1+HP0
1	Y	Sensitivity	XYP1
1	X	Sensitivity	XYP1
0	Z	CrossSensitivity	QP0
0	Y	CrossSensitivity	QP0
0	X	CrossSensitivity	QP0
1	Z	CrossSensitivity	QP1
1	Y	CrossSensitivity	QP1
1	X	CrossSensitivity	QP1

With this magnetic trimming measurement sequence, the following routine has to be implemented:

- Perform several loops with deactivated excitation coils (EC_PO = 0) to get measured values at 25°C.
    - If the measured temperature sensor has a stable value store all values
    - Use the temperature value T0 (at 25°C) for the temperature postprocessing
        - $TOffset = TVal_{T0}$
        - $TValPP_{T0} = TVal_{T0} - TOffset$ should be 0.

- Perform several loops with activated excitation coils (EC_PO = 1) to get measurements at a higher temperature due to self heating
    - Measure the current $ICoil$ at pin VDDHV while operating the excitation coils.
    - Calculate the excitation fields for each coil by
        - $BCoil_{XY} = 191\frac{\mu T}{mA} \times ICoil \times 2$
        - $BCoil_{Z} = 182\frac{\mu T}{mA} \times ICoil \times 2$
    - If the measured temperature sensor has a stable value store the measured values
    - Calculate the postprocessed temperature measurement at T1
        - $TValPP_{T1} = TVal_{T1} - TOffset$

- Calculate all sensitivity related values
    - Calculate the sensor sensitivities at temperature T1
        - $S(TValPP_{T1}) = \frac{BCoil}{HVal_P - HVal_N}$
    - Calculate all $HGainComp$ factors to fit the typical sensitivity functions
        - $HGainComp = \frac{S(TValPP_{T1})}{S_{Typ}(TValPP_{T1})}$

- Calculate all offset related values with postprocessed Hall Measurements HValPP
    - Calculate the sensor offsets at temperature T1 and T0
        - $O_{TValPP_{T1}} = \frac{HVal_{P,T1} + HVal_{N,T1}}{2} \times HConfigFactor \times S_{Typ}(TValPP_{T1}) \times HGainComp$
        - $O_{TValPP_{T0}} = \frac{HVal_{P,T0} + HVal_{N,T0}}{2} \times HConfigFactor \times S_{Typ}(TValPP_{T0}) \times HGainComp$
    - Define all offset over temperature functions
        - $O(TValPP) = O_{TValPP_{T0}} + \frac{O_{TValPP_{T1}} - O_{TValPP_{T0}}}{TValPP_{T1} - TValPP_{T0}} \times TValPP$

- Calculate all orthogonality values
    - Calculate the orthogonality coils fields in Z direction
        - $HValPP_Z = (HValPP_{Z,QP,P} - HValPP_{Z,QP,N})$
    - Calculate the orthogonality coils fields in X any Y direction
        - $HValPP_{XY} = (HValPP_{XY,QP,P} - HValPP_{XY,QP,N})$
    - Calculate the orthogonality compensation factors
        - $Orth_{XY} = \frac{HValPP_{XY}}{HValPP_Z}$

Now the postprocessed Hall value can be calculated according to chapter 6.5.2.

As an example please take a look in the Excel file “Calculation of magnetic trimm values with FH3D04.xlsx”.

7
Digital Building Block

The digital part of the ASIC is separated into four main sub blocks:

- the communication interface with register set
- the state machine for measurement and decimation
- a sequencer for continuous measurement.
- a four byte fuse block (OTP)

The **communication interface** is asynchronous to the state machine. This allows for a fast communication up to 16 MHz.
It reads the serial data via the SPI and provides it as parallel data for the state machine. The measurement output values are written to the SPI so they can be read by the user.
It is important to note that during the communication the SPI clock must not exceed a frequency of 8 times the system clock frequency. Nevertheless, both clock domains are fully static and the clocks can be reduced to 0 Hz.

The **state machine** uses the register content to control the analogue components. It adds up the ΣΔ modulator output values to a decimation value and provides the register set with this data.

The **sequencer** allows the continuous measurement of up to four different sensors using four register 1 configurations.

The **fuse block** contains electrical trim values, the trim data can be read out and applied during startup. Several bits are reserved for customer data.

7.1
Communication Interface

The communication interface is described in detail in chapter 4.1.

7.2
Control State Machine

The digital state machine is a complex building block which controls the analogue components according to the configuration set via the interface, performs measurement cycles and calculates output values from these measurements. The functions are described ‘bottom up’ here. The basic functions are explained first and the complex top level functions in the later chapters. Additional functions not directly involved in the measurement or signal processing algorithms are described last.

7.2.1
Sensor selection and analogue configuration

The state machine uses the parameters for measurement control present in the configuration registers. The sensor is selected according to the setting and the analogue blocks configured. The switching of the hall phase is organized in a non-overlapping way.

Table 46: Decimation enable bit position, register 0x001

Bitpos.	Signal	Meaning
0	DecEn	"Decimation Enable" Setting this bit starts a new measurement. Deleting this bit cancels a running decimation.

7.2.2
Single phase measurement

During a measurement cycle the modulator is controlled according to the number of void cycles and measurement clock periods. The void cycles are necessary to let the analogue front end settle after the change of the hall phase.
The decimation filter computes the output signals of the modulator to a single value. The result from this decimation represents a single phase measurement and can be read via the interface.

Table 47: Decimation length bit position, register 0x001

Bitpos.	Signal	Meaning
7-1	DecLen<7:1>	Decimation Length lower bits DecLen<0> is always 0 If DecLen<10:1> is 0 DecLen = 1 for test modes

Table 48: Decimation length bit position, register 0x002

Bitpos.	Signal	Meaning
10-8	DecLen<10:8>	Decimation Length upper bits DecLen<0> is always 0 If DecLen<10:1> is 0 DecLen = 1 for test modes

Table 49: Decimation wait state bit position, register 0x002

Bitpos.	Signal	Meaning
7-0	DecWait<7:0>	"Decimation Wait states" Number of void clock cycles before the decimation starts, has to be at least 3.

After the measurement is finished, bit Ready in register 0x102 is set and depending on RM<1:0> pin READY goes to high state and the measured value can be read from the result register.

Table 50: Ready flag bit position, register 0x102

Bitpos.	Signal	Meaning
15	Ready	"Decimation Ready" Allows for a polling operation if the READY pin is not connected.

Reading from register 0100h indicates that the measurement result has been read completely and that the internal buffer can be used for the next measurement. If more than one register should be read, the address 0100h must be read last, as it resets the ready signal.

Table 51: Measurement value LSB bit position, register 0x100

Bitpos.	Signal	Meaning
15-0	DecVal<15:0>	"Decimation Value" Measurement value, LSBs

Table 52: Measurement value MSB bit position, register 0x102

Bitpos.	Signal	Meaning
1-0	DecVal<16>	"Decimation Value" Measurement value, MSB

Pin READY can be configured with RM<1:0>. This is necessary if several chips use one ready wire. If only one chip is used ready mode should be set to RM<1:0> = 0x1.

Table 53: READY mode bit position, register 0x005

Bitpos.	Signal	Meaning
2	RM<1>	"Ready Mode" Ready Open Drain 0: pin: push – pull 1: pin: open drain
1	RM<0>	"Ready Mode" Ready Permanent 0: pin high-impedance is CS_N = 1 1: pin always active

7.2.3 Automatic 4-phase measurement

A 4-phase spinning current is needed to reduce the Hall sensors high single phase offsets. The digital state machine switches through the sensor phases and calculates the spinning current value automatically. The digital values from four single phase measurements are added in a configurable way. Together with the single phase offsets, also the offset of the preamplifier is compensated. Such an automatic measurement will result in a value reaching at most four times the maximum of a single phase reading and consume four times the time.
The automatic 4-phase measurement is activated if at least one bit in "Auto4P" is set to 1. The bits Auto4P set the summation scheme. For example for the scheme "-+-+" : 1010.

Table 54: 4-phase summation scheme, register 0x004

Bitpos.	Signal	Meaning
12-9	Auto4P<3:0>	"Automatic 4-Phase spinning signs" Sign order for automatic 4-phase measurement and calibration (standard: 1010).

It is important to note that with activated automatic 4-phase measurement the resulting value can up to decimation length times ±7.5 times 4. Therefore, the MSB must be read if a large decimation length value is set.

In contrast to the hall sensor measurement the temperature measurement uses always only a 2-phase measurement.

7.2.4 Automatic 2-phase measurement

For fast measurements it is possible to activate an automatic 2-phase spinning current. In 2-phase mode the SC-offsets might be a little bit higher.
The 2-phase SC can be activated with bit: Fast2P

Table 55: 2-phase enable bit, register 0x002

Bitpos.	Signal	Meaning
12	Fast2P	"Fast 2-Phase spinning current"

7.2.5 Background Temperature measurement

It is possible to use most of the wait cycles for temperature measurements. During the wait cycles the temperature measurement is activated. If BgndTempMeas<3:0> > 0, BgndTempMeas<3:0> times 4 defines the number of phases which are used to measure the temperature.
Compared to a normal temperature measurement for temperature postprocessing the equivalent decimation length is (DecWait-2)*BGndTempMeas<3:0>*2.
Due to the fact that multiple short time slots are used for sampling the temperature signal instead of two long time slots the accuracy of background temperature measurement is slightly reduced compared to normal temperature measurement.
The corresponding temperature value can be read from register 0x0104.
Attention: Valid data is available after two times BgndTempMeas<3:0> times 4 phases.

Table 56: BgndTempMeas, register 0x00B

Bitpos.	Signal	Meaning
3-0	BgndTempMeas<3:0>	"Background Temperature Measurement"

Table 57: TempVal, register 0x104

Bitpos.	Signal	Meaning
15-0	TempVal<15:0>	"Temperature Value"

7.2.6 Read Value Register 1

If bit RVR1 is set it is possible to read the measurement value from register 0x001 while the new configuration is written to register 0x001. If the measurement is a magnetic four phase or two phase measurement the read value is DecVal[16:1]. If the measurement is a two phase temperature measurement the read value is DecVal[15:0]. If RngWarn is set during the measurement the read value will be 0x7FFF. Rng2Reg100, SeqNr2Reg100, Parity2Reg100 are intended to be 0.

Writing to register 0x001 sets ready to zero if RVR1 is set.

Table 58: RVR1, register 0x005

Bitpos.	Signal	Meaning
0	RVR1	"Read Value Resister 1" Read the decimation value from register 0x001

7.2.7
Parity to Register 100

If bit Rarity2Reg100 is set the parity bit in register 0x0100 is activated.

Table 59: Parity2Reg100, register 0x005

Bitpos.	Signal	Meaning
3	Parity2Reg100	"Parity to register 100"

Parity, SeqNr<1:0> and RngWarn are filled up from the left (MSB) of register 100 with the order: 1st: Parity, 2nd SeqNr<1:0>, 3rd RngWarn.

7.2.8
Sequencer Number to Register 0x100

If bit SeqNr2Reg100 is set the sequencer number bits in register 0x0100 are activated.

Table 60: SeqNr2Reg100, register 0x005

Bitpos.	Signal	Meaning
4	SeqNr2Reg100	"Sequencer number to register 100"

Parity, SeqNr<1:0> and RngWarn are filled up from the left (MSB) of register 100 with the order: 1st: Parity, 2nd SeqNr<1:0>, 3rd RngWarn.

7.2.9
Range Warning to Register 0x100

If bit Rng2Reg100 is set the range warning bit in register 0x0100 is activated.

Table 61: Rng2Reg100, register 0x005

Bitpos.	Signal	Meaning
5	Rng2Reg100	"Parity to register 100"

Parity, SeqNr<1:0> and RngWarn are filled up from the left (MSB) of register 100 with the order: 1st: Parity, 2nd SeqNr<1:0>, 3rd RngWarn.

7.3 Example of a Measuring Process

After the initial reset all registers are set to zero. Now the chip has to be configured. This configuration has to be done only once after the reset.
Now it's possible to start a measurement by choosing the sensor and setting the bit DecEn. Both can be done in register 0x001.
The chip does an automatic 4-phase, 2-phase or 1-phase measurement depending on initial configuration. If the measurement is done the measurement result is transferred into the measurement register and bit Ready in register 0x102 is set and depending on RM<1:0> pin READY goes to high state and the measured value can be read from the result register. By reading the measurement value from register 0x100 bit Ready in register 0x102 and pin READY is set to low.
Now it's possible to start the next measurement.

7.3.1 Continuous measurement

Instead of waiting for a measurement completion and reading the output data before starting a new measurement also a continuous measurement procedure can be used. To enable this, the relevant registers (0x001, 0x002 and 0x003) have shadow registers. This way a new configuration can be written without effecting the configuration of the running measurement. The new configuration is taken over as soon as the running measurement is finished.
Continuous measurement procedure:
If a measurement is started externally before READY indicates the completion of a previous one, the IC triggers the next measurement not before READY goes high. Now the measurement is started internally, and the previous measurement data can be read from the interface. During the decimation the output data can be read, and the next measurement set up, which is again started after the current one is finished.
If a measurement is finished before the previous result is read from register 0100h, the next measurement is not started. It starts after the result is read from 0100h. Directly after that the actual result is available at the output registers.

7.3.2 Offset Centering

For every hall sensor there is a dedicated register to store the offset centering value. During operation these values are regulated towards a minimum single-phase offset. The bit "OCAuto" in register 0x004 enables this function.

The registers are not directly accessible via the interface. Still register 0103h allows for transparent access to the offset centering register of the currently selected sensor. After every automatic 4-phase or 2-phase measurement the offset centering register of the measured sensor is updated with a new value minimizing the single-phase offset.

Table 62: Offset Centering related bit assignment, register 0x004

Bitpos.	Signal	Meaning
8	OCSign	"Offset Centering Sign" Set the regulation direction.
7-6	OCMode<1:0>	"Offset Centering Mode" Assignment of the offset centering values to the phases (standard setting: 10b). AmpOsCM: 10b → Phase 0: AmpOS0_0; Phase 1: AmpOS0_0; Phase 2: AmpOS0_0; Phase 3: AmpOS0_0
5	OCAuto	"Offset Centering Automatic" Enables the offset regulation.
4	OCIRefR	Offset Centering Current Reference Resistor
3	OCToggle	"Offset Centering Toggle" Forces the offset cenreing to toggle between two settings.
2-0	OCGain<2:0>	"Offset Centering Gain" Set the regulation gain for offset centering.

Auto centering is only possible during the automatic 4- or 2 -phase measurement as at least two phases are needed for calculation of the offset centering values. The regulated offset centering values can be read from register 0103h during operation.

Table 63: Offset Centering bit assignment, register 0x010

Bitpos.	Signal	Meaning
7-0	OCVal0<7:0>	„ Offset Centering value 0" The offset centering set value of the next selected sensor.

The regulation works proportionally. In phase 1 and 0 the first 16 summation cycles of the Sigma Delta decimation are used to calculate the difference between two corresponding spinning current phases. An adjustable number of digits of the difference is shifted to the edge and added to the offset centering value.

7.3.3 Control Flags

The FH3D04 has two diagnostic flags which allow for a basic self-monitoring.

RangeWarn indicates that the ADC input value is at the upper or lower limit. The bit is set if during a decimation eight sequenced ADC values are at the upper or lower limit.

HistWarn indicates that there might be an issue with the signal path. The bit is set if during a decimation:

- More than three different ADC values are detected
- Missing ADC value between two ADC values.

Table 64: Diagnostic flag bit positions, register 0x102

Bitpos.	Signal	Meaning
14	HistWarn	"**Hist**ogram **Warn**ing" Indicates an improper distribution of ADC output values inside the possible range.
13	RngWarn	"Range Warning" Indicates that the ADC input signal exceeds the input range.

After a single phase measurement the histogram is available in register 0x103.

Table 65: Bit assignment, register 0x103 for single phase measurements

Bitpos.	Signal	Meaning
14	HistWarn	"**Hist**ogram **Warn**ing" Indicates an improper distribution of ADC output values inside the possible range.

7.4 Sequencer

The sequencer can be used to measure up to four sensors continuously in an endless loop or in a single shot. The sequencer can be enabled in register 0x02F.

Table 66: Sequencer related bit assignment, register 0x02F

Bitpos.	Signal	Meaning
0	SeqEn	“Sequencer Enable“ Endless sequencer measurement. Attention: - Ensure that DecEn in register 0x001 is 0, otherwise sequencer operation will not start. - Ensure pin READY and so bit Ready in register 0x102 is low in before, it will toggle after every sequencer entry

Up to four measurements can be configured in register 0x0030 to 0x033. The content of these registers is copied by the sequencer to register 0x001 like in continuous mode.

Table 67: Sequencer configuration, register 0x030, 0x031, 0x032 and 0x033

Bit-pos.	Signal	Meaning
15-0	Same as register 0x001	Sequencer entry (X) configuration

Only sequencer entrys with DecEn = 1 will be used by the sequencer.

The sequencer does not wait till the last measurement is read from register 0x100. If the last measurement is not yet read the value will be overwritten.

Additionally, the measurement results are written to register 0x130, 0x131, 0x132 and 0x133.

Table 68: Sequencer measurement result, register 0x130, 0x131, 0x132, 0x133

Bit-pos.	Signal	Meaning
15-0	Seq(X)DecVal<15:0>	“Decimation Value“ Measurement value, LSBs

Table 69: Sequencer related registers

Register	Meaning
0x002F	Sequencer enable
0x0030	Sequencer 0 configuration
0x0031	Sequencer 1 configuration
0x0032	Sequencer 2 configuration
0x0033	Sequencer 3 configuration
0x0130	Sequencer 0 decimation value
0x0131	Sequencer 1 decimation value
0x0132	Sequencer 2 decimation value
0x0133	Sequencer 3 decimation value

7.5 Four Byte OTP

The chip has a four byte OTP (fuse) block. It consists of the fuses that hold the data non volatile and a RAM cell. After reset OTP data is read from the fuses to the RAM cells by the OTP state machine automatically.

It contains a lock bit in order to prevent further fuse burning, it can be burned by customer (e.g. after finishing customer module end-of-line test). Additionally the OTP stores electrical trim values (BGTrim<5:0>, IBiasTrim<4:0> and SRegTrim<3:0>) gathered during semiconductor production test. Several bits can be used by customer (e.g. for serial number).
The OTP block is organized in 4 bytes located at the OTP addresses 0x80 to 0x83. OTP Address 0xFF is reserved for the control register.
The interface to access the OTP via SPI is done with OTP address-register at SPI register 0x050 and OTP data register at SPI register 0x051.

Table 70: OTP adress register bit assignment, SPI register 0x050

Bitpos.	Signal	Meaning
15-8	Reserved	Reserved set to zero
7-0	OTPAddr<7:0>	OTP Address 0x80: Byte 0 0x81: Byte 1 0x82: Byte 2 0x83: Byte 3 0xFF: Control register

Table 71: OTP data register bit assignment, SPI register 0x051

Bitpos.	Signal	Meaning
15-8	Reserved	Reserved set to zero
7-0	FuseData<7:0>	Fuse Data

If one of the fuse bytes is addressed, the corresponding RAM cells can be read or written. If the Control-Register is addressed, several modes can be activated.

Table 72: OTP register 0xFF (Control register) bit assignment

Bitpos.	Signal	Meaning
7-0	P2RAMControl	P2RAM Control

Commands for the P2RAM_Control:

0x00	EXIT_CMD	Disables access to P2RAM
0x08	BURN_CMD	A further write starts burning of the fuses
0xFD	FOUNDRY_CMD	Enables access to P2RAM (Read and write RAM)

Attention: Fuse programming is only allowed with the nominal system clock frequency of 8 MHz!
Attention: Fuse programming draws about 100 mA for a short time. Ensure that the supply system is able to provide this current. Do not program more than one bit at once, program bit by bit to let supply recover from current spike.
The completion of the internal programming procedure is signalized by pin Ready.

Table 73: OTP Byte 0, OTP register 0x80 bit assignment

Bitpos.	Signal	Meaning
7-0	tbd	Customer area

Table 74: OTP Byte 1, OTP register 0x81 bit assignment

Bitpos.	Signal	Meaning
7-1	tbd	Customer area
0	SRegTrim<0>	Trim data for sensor regulator

Table 75: OTP Byte 2, OTP register 0x82 bit assignment

Bitpos.	Signal	Meaning
7-3	IBiasTrim<4:0>	Trim data for IBias generation
2-0	SRegTrim<3:1>	Trim data for sensor regulator

Table 76: OTP Byte 3, OTP register 0x83 bit assignment

Bitpos.	Signal	Meaning
7	LockDaisy	Lock Daisy Chain, always 1
6	LockOTP	Lock OTP
5 – 0	BGTrim<5:0>	Trim data for Bandgap

7.5.1 OTP read example

Read OTP Byte 3 content:

- **8050h – 0083h** and **8051h – 0000h**
  - Request content of fuse byte 3 and read fuse data.

7.5.2 OTP programming example

Program OTP Byte 0 Bit 0 with 1b:

- **8050h – 00FFh** and **8051h – 00FDh**
  - Enables access to the P2RAM
- **8050h – 0081h** and **8051h – 0001h**
  - Store 0x01 in the RAM cell of byte 1
- **8050h – 00FFh** and **8051h – 0008h**
  - Set fuse block in programming mode
- **8050h – 0081h** and **8051h – 00xxh**
  - another write to byte 1 starts the programming (xx don't care)
- **8050h – 00FFh** and **8051h – 0000h**
  - Disables access to P2RAM

After a reset the new OTP content is available for read.

8 Detailed Building Block Description

8.1 Block Enable / Disable

The main building blocks in the design can be enabled separately. Thus the IC can be set to inactive modes to reduce power consumption during operation.
All power on bits are located in register 0x006.

8.2 Reset_N

During or at least after rise of the supply voltage (power on), pin RESET_N has to be set to 0 V to reset the chip. The reset affects the interface and the state machine. It is fed through directly to all registers and is released synchronized to a system clock edge.

8.3 References

An internal bandgap reference generates a constant voltage from which bias currents, excitation coil current, and the ADC references emerge. The bias current is generated with an integrated shunt.
Additionally, a temperature dependent signal is generated.

Table 77: References

Parameter	Min.	Typ.	Max.	Unit	Note
Positive ADC Reference Voltage		2.1		V	
Negative ADC Reference Voltage		0.9		V	
Bandgap Reference Voltage		1.2		V	Trim value stored in OTP, need to be read out and applied to register 0x040 during initialization. Customer specific trim possible during module End-of-Line test.
Bias current		10.0		µA	Trim value stored in OTP, need to be read out and applied to register 0x040 during initialization. Customer specific trim possible during module End-of-Line test.

The references block can be controlled by the following bits.

Table 78: References setting bit position, register 0x006

Bitpos.	Signal	Meaning
6	Bias_PO	“Bias Power On“ Switch on the internal bandgap reference.

Table 79: References setting bit position, register 0x040

Bitpos.	Signal	Meaning
14-9	BGTrim<5:0>	“Bandgap Voltage Trimming”
8-4	IBiasTrim<4:0>	“Bias Current Trimming

Table 80: References setting bit position, register 0x008

Bitpos.	Signal	Meaning
12	IBBoostOC	“Bias Current Boost Offset Centering”
11	IBBoostModRefBuf	“Bias Current Boost Modulator Reference Buffer”
10	IBBoostBUF	“Bias Current Boost Buffer”
9	IBBoostEC	“Bias Current Boost Excitation Current”
8	IBBoostMod	“Bias Current Boost Modulator”
7	IBBoostPGA	“Bias Current Boost PGA”
6	IBBoostSReg	“Bias Current Boost Sensor Regulator”

Increasing IBiasTrim compared to the trim value stored in OTP will decrease the bias current for all blocks and lower the overall power consumption. Some analog blocks might need additional bias current for proper operation. The IBBiasBoost bits add about 2µA additional bias current to the corresponding analog block. This way it is possible to increase the bias current of a single block during low power mode.

8.4 Sensors

Four pixel cells, each with an X-/Y-/Z-Sensor, are arranged in a square with a pitch of 1.5mm.

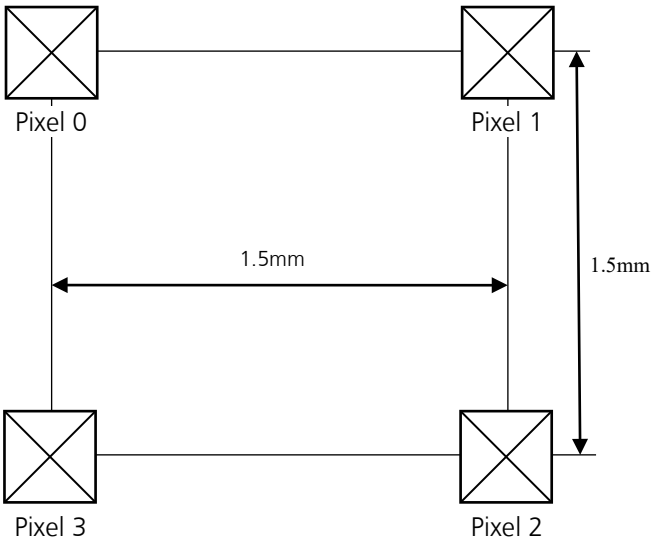

Figure 14: Pixel cell arrangement

The sensor sensitivity, current consumption and offsets vary from chip to chip and over temperature. The sensor parameters are normalized to the sensor supply voltage of 2.6 V.

Table 81: Hall sensor sensitivity and resistance

Parameter	Min.	Typ.	Max.	Unit	Note
Sensitivity X-/Y-sensor		54		mV/T	at 2.6 V sensor supply voltage, 25°C
Sensitivity Z-sensor		95		mV/T	
Resistance X-/Y-sensor		850		Ω	
Resistance Z-sensor		1135		Ω	

The exact position on silicon chip according to design database:

P0: 485 µm / 1985 µm P1: 1985 µm / 1985 µm

P2: 1985 µm / 485 µm P3: 485 µm / 485 µm

8.5 Sensor multiplexer

The sensor multiplexer activates the desired pixel cell, sensor type and phase.

The configuration bits are present in register 0x001, 0x002 and 0x004.

Table 82: Sensor setting bit position, register 0x001

Bitpos.	Signal	Meaning
11-10	PixelSel<1:0>	“Pixel Select” Pixel 0 [00b], Pixel 1 [01b] Pixel 2 [10b], Pixel 3 [11b]
9-8	SensSel<1:0>	“Sensor Select” X [00b], Y [01b], Z [10b] [11b] deactivates the hall sensor during temperatura measurement

Table 83: Sensor setting bit position, register 0x003

Bitpos.	Signal	Meaning
1-0	Phase<1:0>	“Phase setting” Sets the spinning current phase for all sensors.

The sensors need to be enabled to output a signal. The supply and sensor output can be enabled separately. Without the sensor output enable the preamplifiers input is floating.

Table 84: Sensor enable bit position, register 0x006

Bitpos.	Signal	Meaning
1	SMUXPowEn	“Sensor-Multiplexer Power Enable“ Enable of the sensor supply transistors.
0	SMUXSigEn	“Sensor-Multiplexer Signal Enable“ Enable the transmission gates between sensor output and preamplifier.

An additional bit allow the configuration of the sensor multiplexer. SMUXChopInv inverts the analog sensor signal. Additionally the digital measurement value is inverted. This way it is possible to choose the best combination of sensor offset and PGA offset in order to get the biggest measurement range.

Table 85: Sensor setting bit position, register 0x002

Bitpos.	Signal	Meaning
11	SMUXChopInv	“Sensor-Multiplexer Chopper Invert“ Inverts the Hall signal for offset compensation.

8.6 Sensor Supply Voltage Regulator

The sensor supply voltage can be controlled by an integrated supply regulator. The voltage of the negative supply node UN and the differential sensor supply voltage UD can be set, both present in register 0x003. Additionally, the sensor supply voltage can be trimmed via SRegTrim<3:0> in register 0x040. The corresponding trim value is stored in OTP.
If the signals SRegN_PO and SRegD_PO (register 0x004) are deactivated, the sensors are directly connected to VDD and VSS.

Table 86: Sensor supply regulator settings

SMPowEN	SRegNPO	SRegDPn	Sensor supply	
			Low supply	High supply
0	X	X	off	off
1	0	0	VSS	VDD
1	0	1	VSS	regulated
1	1	0	regulated	VDD
1	1	1	regulated	regulated

The voltages at the supply nodes affect all sensors identically.
With sensor supply voltage regulator enabled six modes of operation can be selected.

Table 87: Sensor Supply modes

Mode	UN	SRegNVal	UD	SRegDVal
Standard (Default)	0.2 V	0	2.6 V	5
Low offset	0.5 V	2	2.0 V	3
High sensitivity (VDD > 3.2 V)	0.2 V	0	2.8 V	6
Half sensitivity	0.65 V	3	1.3 V	2
Quarter sensitivity	0.95 V	5	0.65 V	1
Eighth sensitivity	1.1 V	6	0.325 V	0

UN: negative sensor supply node

UD: differential sensor supply voltage

The sensor supply voltages must be set to a reasonable value matching to the input range of the pre-amplifier. Note that the differential supply voltage is critical for the sensors sensitivity.

Table 88: Sensor supply bit position, register 0x006

Bitpos.	Signal	Meaning
3	SRegN_PO	"Sensor supply voltage Regulator Negative Power On" 1: lower supply voltage is regulated, 0: power off for lower supply voltage => if SMPowEN = [1], then the sensor connected directly to VSS
2	SRegD_PO	"Sensor supply voltage Regulator Differential Power On" Activates the regulator for the sensor supply voltage. 1: differential supply voltage is regulated, 0: power off for differential supply voltage regulator => if SMPowEN = [1], then the sensor is connected directly to VDD

Table 89: Sensor supply bit position, register 0x003

Bitpos.	Signal	Meaning
15-13	SRegDVal<2:0>	"Sensory supply voltage Regulator Differential Value"
12-10	SRegNVal<2:0>	"Sensor supply voltage Regulator Negative Value"

Table 90: Sensor supply bit position, register 0x040

Bitpos.	Signal	Meaning	Note
3-0	SRegTrim<3:0>	"Sensor Regulator Voltage Trimming"	Trim value stored in OTP, need to be read out and applied to register 0x040 during initialization. Customer specific trim possible during module End-of-Line test.

The supply voltage regulator is separated into two sub blocks:
SupRegSetPoint generates the analogue set point for the regulators
SupReg contains the opamps which regulate the voltage at the negative and positive supply to the defined voltages

The set point DAC translates the digital input to analogue reference output values for the sensor supply regulator.
Depending on the 1.2 V bandgap reference voltage and the operational amplifier offset the sensor supply voltages have limited accuracy. To increase the accuracy, the set point DAC is trimmed.

8.7 Excitation Coil and Current DAC

Every sensor is magnetically coupled to an excitation coil which can apply a magnetic field to the sensors. The current through this coil is generated by a 3-bit current DAC, whose digit converts into a current I0, typically 100 µA. The output stage can work in a low voltage and high voltage mode, where the output current is multiplied by 2 or 14. This results in a current range from typically 0.2 to 1.6 mA in the low voltage mode and from 1.4 to 11.2 mA in the high voltage mode.

EnHV=0: current=0.2 mA x (ECVal<2:0> + 1)
EnHV=1: current=1.4 mA x (ECVal<2:0> + 1)

Due to the orientation of the sensors two different coils are necessary to apply magnetic fields to the vertical and horizontal sensors.

Two additional coils are placed to enable distance measurements between coil and sensor and cross sensitivity measurements between X- and Y- to Z- sensors.
The physical width of the coil metal wires is only 0.95 µm at the narrowest point. According to the design rules the maximum allowed dc current is 0.63 mA at 125°C. Because the coils are used in AC mode, higher currents can be applied during the routine test of the chip.

Table 91: Excitation coil parameters, measured on a small number of samples

Parameter	Min.	Typ.	Max.	Unit
Coil factor X- and Y-sensor		187.1		µT/mA
Coil factor Z-sensor		178.8		µT/mA
Calibration coil factor X- and Y-sensor	115		160	µT/mA
Cross sensitivity X- and Y-sensor		0		µT/mA
Current per digit; ENHV = 0		0.2		mA
Current per digit; ENHV = 1		1.4		mA

Table 92: Current source power on bit position, register 0x006

Bitpos.	Signal	Meaning
7	EC_PO	„Excitation Current Power On“ Switch on the excitation current source.

Table 93: Excitation current setting bit position, register 0x003

Bitpos.	Signal	Meaning
9-6	ECCSel<2:0>	„Excitation Current Coil Select“ Activates the calibration coil. 0: coils off 1: P2 XY 2: P2 Q 3: P2 Z + P1 H 4: P2 H + P1 Z 5: P1 Q 6: P1 XY 7: P3 XY 8: P3 Q 9: P3 Z + P0 H 10: P3 H + P0 Z 11: P0 Q 12: P0 XY
5-3	ECVal<2:0>	„Excitation Curent Value“
2	ECSign	“Excitation Current Sign“ Direction of the excitation current.
13	ECEnHV	“Excitation Current Enable High Voltage“ Enables the high voltage mode

Table 94: Current source HV enable bit position, register 0x004

Bitpos.	Signal	Meaning
13	ECEnHV	“Excitation Current Enable High Voltage“ Enables the high voltage mode

Due to the rotations of the pixels the excitation coils have the following signs:

Table 95: Excitation of the single sensors

Coil type	Pixel 0	Pixel 1	Pixel 2	Pixel 3
XY	X: + Y: +	X: - Y: +	X: - Y: -	X: + Y: +
Z	Z: -	Z: +	Z: -	Z: -
Q	Z: -	Z: +	Z: -	Z: -
H	X: + Y: +	X: - Y: +	X: - Y: -	X: + Y: +

8.8 Temperature Measurement

The chip contains a linear temperature sensor. A separate buffer provides the ADC with the appropriate signal strength. The intrinsic buffer offset is eliminated by automatic chopping the input signal.
The measurement is treated like a normal signal reading where the temperature sensor represents a special sensor. It can be activated by selecting bit TempSel.
Please note, that even with inverted input signals the temperature output signal is not inverted but only shifted by the intrinsic offset. This allows for a quasi-calibration measurement on the temperature sensor with an offset free result.

Table 96: Temperature sensor select bit position, register 0x001

Bitpos.	Signal	Meaning
12	TempSel	"Temperature Select" Select the temperature sensor.

8.9 Programmable Gain Amplifier

Single stage analogue low-noise instrument amplifier with gain steps of 32, 64, 128, 256, 512 and 1024. For very large magnetic fields, the sensor supply and hence the sensor sensitivity can be reduced.

Table 97: Amplifier power on bit position, register 0x006

Bitpos.	Signal	Meaning
4	Amp_PO	"Amplifier Power On" Switch on the preamplifier.

Table 98: Amplifier gain, register 0x001

Bitpos.	Signal	Meaning
15-13	AmpGain<2:0>	"Amplifier Gain" Set the Gain.

Table 99: Amplifier compensation, register 0x002

Bitpos.	Signal	Meaning
15-13	AmpComp<2:0>	"Amplifier Gain" Set the Miller compensation to change the bandwidth. If AmpComp = 7 the auto compensation is activated which leads to a typical bandwith of 1.2 MHz.

Table 100: PGA parameters

Parameter	Min.	Typ.	Max.	Unit
Gain in setting 000		32		V/V
Gain in setting 001		64		V/V
Gain in setting 010		128		V/V
Gain in setting 011		256		V/V
Gain in setting 100		512		V/V
Gain in setting 101		1024		V/V

8.10 Offset-Centering

This mechanism allows for the use of a large input range of the ADC even if the single phase offset of the Hall sensors is large. An additional offset is applied to the sensor output compensating for a better part of it. Every sensor needs its own offset values for compensation. They are regulated automatically or can be set manually.

The offset centering is realized as a current source which is connected to the sensor. Depending on the sign its effect is positive or negative.

The control word is 8 bit signed integer.

If the centering current is derived from the sensor current, the step size is independent of the sensors resistance.

Table 101: Offset centering parameters

Parameter	Min.	Typ.	Max.	Unit
Generated offset voltage per digit		200		µV

The offset centering can be operated manually or in an automatic mode. The automatic mode is described in chapter 7.3.2.

Table 102: Offset Centering power on bit position, register 0x006

Bitpos.	Signal	Meaning
10	OC_PO	"Offset Centering Power On " Switch on the offset centering.

Table 103: Offset Centering values, register 0x010

Bitpos.	Signal	Meaning
7-0	OCVal0<7:0>	"Offset Centering Value 0" The values are used for offset centering.

Due to the internal wiring this register is not applied directly after writing but only if a measurement is started (bit 0 in register 0001h). Additionally, the configuration must not be written a second time before starting the measurement. Otherwise it would not be applied. There is one further way to generate the centering current which can be configured in register 0x004.

Table 104: Offset Centring current source, register 0x004 content

Bitpos.	Signal	Meaning
4	OCIRefR	Offset Centering Current Reference Resistor 0: Use external sensor voltage control current 1: Use reference / replica resistor generated current

8.11 Buffer

As the PGA itself cannot drive the switched capacitor circuitry of the ADC, additional buffers are needed between the two blocks. The buffer gain is typically 1.
The buffer works as multiplexer to switch between magnetic signal and temperature signal. As the temperature signal has a much lower voltage the input type is PMOS in, whereas the magnetic signal input type is NMOS. The input is switched automatically depending on the activated sensor.

Table 105: Buffer power on bit position, register 0x006

Bitpos.	Signal	Meaning
8	Buf_PO	"Buffer Power On" Enables the ADC buffers between PGA and ADC.

The input selection is automatically done by choosing the temperature sensor.

Table 106: Choosing the temperature Sensor 0x001

Bitpos.	Signal	Meaning
12	TempSel	"Temperature Select" Select the temperature sensor.

8.12 Sigma-Delta Modulator

The Sigma-Delta-Modulator converts the analogue values into digital data. It can be clocked with a maximum frequency of 8 MHz at the most. With the 4-bit topology and the decimation length register width of 11 bit the maximum possible resolution is 15 bit. The modulator input is fully differential. Positive and negative signals symmetrical to 0.

Table 107: Modulator power on bit position, register 0x006

Bitpos.	Signal	Meaning
9	ModRefBuf_PO	"Modulator Reference Buffer Power On" Switch on the reference buffer
5	Mod_PO	"Modulator Power On" Switch on the ADC.

At the beginning of a measurement the input signal has to settle so that the first ADC codes are correct. A void cycle counter allows the analogue signal to settle after a new measurement cycle is triggered. See setting DecWait in register 002h.

8.13 System Clock

The system clock has to be fed in via the dedicated CLK pad. The typical clock frequency is 8 MHz. Any floating state of CLK has to be prevented.
The SPI interface is independent from the system clock and can be controlled asynchronously.

Table 108: System clock parameters

Parameter	Min.	Typ.	Max.	Unit	Note
Typical CLK frequency	7.95	8.0	8.05	MHz	The characterization of the chip was done with a frequency 8 MHz.
Maximum frequency range	1.0	8.0	8.05	MHz	
Duty Cycle	49	50	51	%	

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